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P 2000 C

SYSTEM REFERENCE AND SERVICE MANUAL

First reprint week 417 (incorporating AL 1)

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Philips Portable Computer







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Introduction

INTRODUCTION

With the introduction of the Philips P2000C, it is now possible to have a complete computer system in one easily portable package; including a keyboard, a monitor and two floppy disk drives.

This 8 bit, 64 kbyte personal computer has the following features:

- compact design
- portable
- dual processor 8 bit, 64 kbytes CPU RAM 32 kbytes VID RAM
- built-in 9" monochrome green CRT
- 320 or 1280 kbytes mass storage (2 built-in floppy disks)
- choice of operating systems

CP/M

p-System (Pascal)

- optional RAM-Board (256 kbytes)
- optional IEEE board

Combining portability with the latest in computer design techniques the P2000C allows the user to make a choice of operating language and to select, from the complete internal character set, a sub-set that suits his particular needs at any moment. This character set can easily be changed at any time.

Built up on two printed circuits, one being the 'computer' the other the 'terminal' and integrated with the built-in monitor and disk drives, the P2000C comes as a complete system but allows additional units to be connected. Peripheral devices that may be added include:

- printer
- external monitor
- V24 communication device (modem)
- external 5½" floppy disk drives
- hard disk or 8" floppy disk via SASI

The Mainboard 'computer' of the P2000C can be used in conjunction with an external terminal and the 'Terminalboard' can be used as an Intelligent Terminal.

Introduction



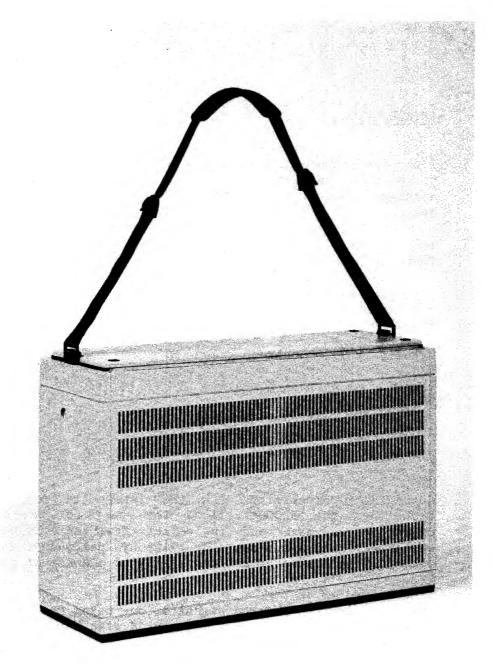


Figure 1.1 The P2000C Portable Computer



RELATED DOCUMENTS

CP/M Users Guide CP/M Reference Manual

IEC Publication 435, Draft 1983 ÖVE-EM 42 Parts 1 and 2

Z80A Data Sheets: Mostek 1979 Microcomputer Components
Data Sheets
Intel Component Data Catalogue 1981
ANSI Document X3T9.3 No.185 - Shugart Associates System
Interface (SASI)
NEC uPd Floppy Disk Controller Data Sheet

TEAC FD 55 A Floppy Disk Drive Specification
Doc. No. P/N 10530146-00 B

TEAC FD 55 F Floppy Disk Drive Specification
Doc. No. P/N 10530146-03 A

Mitsubishi 9" Monitor NT-1002XU Specification

Introduction



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Operating Systems ${\sf CP/M}$

1 GENERAL

No attempt will be made in this manual to describe the standard CP/M operating system, as this subject is suitably covered in existing documents. The following documents are recommended:

- CP/M USERS GUIDE (supplied with the P2000C)
- CP/M REFERENCE MANUAL

Operating Systems $\operatorname{CP/M}$



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Operating Systems p-System

1 GENERAL

No attempt will be made in this manual to describe the standard p-System operation, as this subject is suitably covered in the relevant documentation.

Operating Systems p-System



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Operating Systems
Basic I/O System (BIOS)

1 GENERAL

The two Operating Systems currently available are:

- CP/M[#] 2.2; - p-Systems * 4.1-2

and are used with the Basic Input Output System (BIOS).

The 4 KBytes System PROM (I P L PROM) contains:

- the initial loading program
- the drivers for the peripheral devices
- a memory and peripheral debugger for maintenance purposes

2 INITIAL PROGRAM LOAD (IPL)

The sequence of events during IPL is as follows:

- Port Initialization
- Transfer part of device drivers to RAM
- Initial handshake with the terminal board
- Initialization of floppy controller
- Load system track(s) from floppy or hard disk

These events are described below.

2.1 Port Initialization

The ports are initialized as follows:

- Reset for SASI controller.
- CTC1 channel-0 supplies 19200 x 16 Hz for SIO-B (terminal).

 channel-1 supplies 9600 x 32 Hz for SIO-A (comms).

 channel-2 supplies 1200 x 16 Hz for USART (printer).

 channel-3 is programmed as DMA interrupt device.
- * Trademark of Softech Microsystems
- # Trademark of Digital Research Inc.

Operating Systems Basic I/O System (BIOS)



- CTC2 channel-0 generates the 60 Hz timer interrupts. channel-1 generates 2400 Hz for channel-0. channel-2 is not initialized (reserved for extensions). channel-3 is the interrupt device for floppy and SASI.
 - SIO channel-A is a polled asynchronous communication device. channel-B is programmed for DMA output and interrupt driven input for the terminal interface.
 - USART is programmed as an 1200 Baud output device for the printer.
- Floppy controller is reset.

2.2 Transfer (part of) Device Drivers to RAM

The following blocks are transferred:

- Jump table for the console status, console input, console output, list output, communication output and communication input subroutines to address F606. This table is followed by the memory disk initialization program.
- The RAM resident part of the device driver subroutines and the corresponding tables that have to be initialized.
- Table of interrupt vectors to address FFDO.

2.3 Initial Handshake with the Terminal Board

Two characters are expected from the terminal board and they are immediately returned. No further operation takes place until this handshake is completed. If this handshake is not completed successfully, the message 'SYSTEM ERROR' is displayed by the terminal program.

2.4 Compute ROM Checksum

All bytes in the ROM from O to FFD are added in a two byte long word and compared with the value stored in FFE and FFF. If no match is found, the message BAD ROM is displayed and the program stops, otherwise the IPL version number is displayed. (e.g., 'IPL-1.1').



Operating Systems Basic I/O System (BIOS)

2.5 Initialize the Floppy Controller

If the ready bit of the floppy controller is not set the system ignores all further floppy commands (the SASI interface remains active).

If the ready bit of the floppy controller is set, a wait loop is started until the first interrupt from the floppy controller is sensed. A SPECIFY command is then issued with the following values:

- Step rate time = 6 ms
- Head unload time = 480 ms
- Head load time = 5 ms

2.6 Load System Track(s) from Floppy or Hard Disk

An attempt is made to read side-0 track-0 from floppy-1 to D600. If no valid data is obtained, HARD DISK-1 and then floppy-2 are read. If unsuccessful, the message "SYSTEM DISK?" is displayed and the user can depress any key (except ESC) to repeat the procedure.

When the first track (side-0 track-0) has been loaded, the following data structure is expected:

	-	0, 1, 2:		Jump to continue program
_	Byte	3:	80H	Load only one track
			81H	Load the second track from side-0
				track-1
			82H	Load the second track from side-1
				track-0
_	Byte	4:	PB	Printer baud rate byte
_	Byte	5:	CB	Communication baud rate byte
_	Byte	6:	SR	Floppy step rate byte
	-,		ODO	For 6ms (system with 160K drives
				or mixed drives)
			0EO	For 4ms (system with 640K drives
				only)

If byte-3 is not in the range 80 - 82H, the track is considered as invalid.

If a valid IPL track-0 is read, and Byte-3 is 81 or 82H, then the second track is read to E600.

The baud rate bytes (4 and 5) are:

Speed 75 150 300 600 1200 2400 4800 9600 19200 Byte 0 80H 40H 20H 10H 08H 04H 02H 01H

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The printer and communication speeds are then corrected according to Bytes 4 and 5, the floppy step rate is updated according to byte 6 and a jump is made to the extension RAM initialization program.

The extension RAM (which may be fitted as an option - see Chapter 7) is expected to be used as a RAM disk and therefore its directory range must be cleared after reset.

After the RAM disk initialization the 4 system clock bytes are also cleared.

If the user wants to preserve the information on the memory disk and the system clock, he must depress the SPACE bar during RESET and hold it down for at least 5 seconds.

Note: Generally, information on the memory disk will not be changed but it is stressed that this cannot be guaranteed.

The memory manager is then switched to RAM operation, the extension RAM is switched off and the program is continued on D600 i.e., the first user supplied instruction.

The BOOTDR byte (Byte 1AH in DPB - Driver Parameter Block) contains the address of the booting device:

0: floppy-1 1: floppy-2 FF: hard disk

3 DRIVERS FOR THE PERIPHERAL DEVICES

The peripheral drivers are located partly in the System ROM, partly in the highest part of the RAM. The entry points are always in RAM and can be accessed either from the loaded jumping table or from the Driver Paramater Block. The address of the Driver Parameter Block is stored at FFDOH.

EXAMPLE

To use the disk-read routine:

READ:LD	HL, (OFFDOH)	;addr of parameters block
LD	DE,9	offset in the DPB .
ADD	HL, DE	
LD	E,(HL)	
INC	HL	
LD	H,(HL)	
LD	L,E	;HL has the ADDRESS OF RDS
JP	(HL)	jump to read subroutine

This sequence can be used, of course, only as CALL READ.



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3.1 Driver Jumping Table

The jumping table loaded by the IPL starts at address F606. It can be overwritten by the loaded operating system after the required addresses are patched into the CBIOS or SBIOS.

The first jump instruction in this table is directed to the Console Status subroutine. The address of this sub-routine is also the first address used by the system.

The table contains the following items:

3.1.1 CONSOLE STATUS

F606: JMP CONST

Action: the value of KSTAT (byte 27H in DPB) is read. On exit: A = FF and zero flag is reset if any key input

A = 0 and zero flag is set if no key input

all other registers are unchanged.

3.1.2 CONSOLE INPUT

F609: JMP CONIN

Action: wait until KSTAT is non-zero

clear KSTAT

enable next keyboard interrupt

if SIO contains no further characters, set the DTR

line

get KBYTE (byte 28H in DPB) into the accumulator. (In the keyboard interrupt subroutine the KSTAT byte is set to FF and the DTR line on the SIO is reset.)

On exit: A = input character

registers H and L are lost, all other registers are

unchanged.

For details of the caps lock function see the description of the terminal board software.

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CONSOLE OUTPUT 3.1.3

F6OC: JMP CONOUT

On entry: register C contains the character to be output. wait until a place is free in the 40H bytes long TTOBUF field and put the character on the first free buffer position; if it is the first position in the buffer, start DMA transfer.

> Note: (If a DMA transfer is ready, a DMA interrupt is generated. The interrupt service routine checks if any characters are waiting in the buffer for sending. If so, these characters are shifted to the start of the buffer and the next DMA transfer is started. The buffer pointer is set to the first free position. As a result, other operations can be done by the system during terminal transfer because it does not have to wait for transmission ready.)

On exit: All registers except A are unchanged.

LIST (PRINTER) OUTPUT: 3.1.4

F60F: JMP LIST1

On entry: register C contains the character to be printed. the PRTAB word (Bytes 15H & 16H in DPB) is checked.

- the character is printed without change. If nonzero - it is the address of the printer table. (Its structure is described in the CP/M Reference Manual in the section dealing with the Configuration Program). If the character is found in the table, it is table value(s), the replaced bу otherwise it is printed without change. If a character is not found in the

printer table and its'

9FH, a space (20H) is printed. This saves some bytes in the printer table.

404

value is over



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If both the printer and the USART are ready, the character is printed immediately, otherwise the PRSTAT byte (Byte 18H in DPB) is checked.

an error return is made immediately.

If nonzero - the PRWAIT byte (Byte 17H in DPB) is checked. It defines the maximum waiting time in 4 second units, however a value of 4 can mean a waiting time between 12 and 16 seconds. During the wait loop, repeated attempts are made to print. In the event of a timeout the PRCONT byte (Byte 19H in DPB) is checked.

an error return is made. If zero -

If nonzero - the message 'IGNORE PRINTER WITH ESC' is displayed and the next console input is checked. If 'ESC' an error return is made, otherwise the checking of the ready bit is repeated.

On exit: if print was successful, register A and PRSTAT = FF and zero flag reset.

if printer error, register A and PRSTAT are 0 and

zero flag is set.

Registers B,C,D,E,H and L are lost.

COMMUNICATION (PUNCH) OUTPUT 3.1.5

F612: CALL COMOJP

On entry: register C contains the character to be sent.

waits until the SIO-A transmitter is ready and then Action:

sends the character.

On exit: registers A, H and L are lost.

COMMUNICATION (PUNCH) INPUT: 3.1.6

F615: CALL COMIJP

wait until the SIO-A receiver is ready and then fetch Action:

the character.

register A holds the received character. On exit:

registers H and L are lost.

Operating Systems Basic I/O System (BIOS)



3.2 Routines Defined by the Driver Parameter Block (DPB)

The address of the Driver Parameter Block is stored at FFDO-FFD1. (It is the first address in the interrupt vector table, but the corresponding channel never interrupts). The subroutine addresses defined in this block must be patched into the operating system after program load.

3.2.1 READ ONE OR MORE SECTORS FROM DISK

Bytes 09-OAH: DEFW RDS

On entry: Bytes 0 - 8 of the DPB must be correct.

Byte 0: DRIVE - defines the selected drive.

Values: 00H floppy-1

01H floppy-2

02H floppy-3

03H floppy-4

10H memory disk

FFH hard disk-1

FEH hard disk-2

Bytes 1 & 2: TRACK - defines the selected track, low byte on 1, high byte on 2. The ranges:

0 to 27H (39) for single track

0 to 4FH (79) for double track

0 to 3FH (63) for memory disk

0 to 4C7H (1223) for 5 MB hard disk

A track length of 4 kbytes is assumed.

Byte 3: SECTOR - defines the selected sector

Range: 1 - 10H

Byte 4: HEAD - defines which side of floppy is taken

0 for side - 0

1 for side - 1

Byte 5 & 6: RWBUFF - defines the address of read or write data

Byte 7 & 8: RWLGTH - is transfer length-1 (FFH for 1 sect, OFFFH for 1 track). For floppy and memory disk transfer the operation must not extend over the track limit. For hard disk the maximum value is 3FFFH.



Operating Systems
Basic I/O System (BIOS)

Action - Floppy Calls:

If the NOFLOP flag is set (floppy controller not ready after initialization), an error return is made. If the floppy controller is present, the motor is switched on if not already running. A seek is made to the required track if different to the previous access. The floppy controller parameter block is filled in. A call is made to DSKTR (DPB + 1FH). If this location has 0 (NOP), standard numbering is expected, if 24H (INC H), an old PHILIPS format is selected (track-0 is numbered with 1). The controller is then activated.

The transfer is carried out under DMA control. If an error has been found, the procedure is attempted 8 times, the head is stepped out 10 tracks if TRACK is less than 10, the controller is recalibrated, a seek is made to the track and 8 new attempts are made. If not successful, an error return is made. No repeat is made if 'disk not ready' is found or if the disk is write protected.

Action - Hard Disk Calls:

The XEBEC parameter block is filled in. The SASI controller ready bit is checked and, if not ready, an error return is made.

The DMA is programmed for transfer, and the XEBEC parameter block is transmitted. If an error is found, the hard disk error subroutine (HDERSU from DPB bytes 1D-1EH) is called (it is an empty program, for maintenance purposes only), the controller is reset and the procedure is repeated.

After a floppy or hard disk operation the DMA is checked for transfer length to avoid incorrect transfers. In case of error the operation is repeated according to the repetition algorithm.

Action - Memory Disk Calls:

IMPORTANT WARNING: RWBUFF MUST ALWAYS HAVE AN ADDRESS OVER 8000H!!!

The selected track number and the existence of the extended memory is checked. If OK, the corresponding cache block is switched and the transfer is made.

On exit: A = O and zero flag is set if operation OK, otherwise A = FF and zero flag is reset.

Registers HL DE and BC are destroyed.

The DPB bytes O to 8 are not changed! In case of floppy calls the RESULT field (DPB bytes 2D to 33H) contains the controller result bytes.

Operating Systems Basic I/O System (BIOS)



3.2.2 WRITE ONE OR MORE SECTORS TO DISK

Bytes OB-OCH: DEFW WRS

All interfaces are identical to the READ subroutine.

3.2.3 STEP TO A TRACK (floppy only)

Bytes OD-OEH: DEFW STEP

The given address is the System ROM address of the stepping routine, therefore the System ROM must be switched on before calling. Its use is not recommended except for maintenance purposes.

On entry: DRIVE and TRACK in DPB must be filled.

Action: if the selected drive and track are identical with

the previous ones, nothing is done. If the present track position is undefined, a RECALIBRATE precedes

the SEEK operation.

On exit: all simple registers are destroyed.

3.2.4 RECALIBRATE DRIVE (floppy only)

Bytes OF-10H: DEFW RECAL

The given address is the system ROM address of the recalibrate routine, therefore the system ROM must be switched on before calling. Its use is not recommended except for maintenance purposes.

On entry: DRIVE in DPB must be filled.

Action: the selected drive is recalibrated (stepped to

track-0).

On exit: all simple registers are destroyed.



Operating Systems Basic I/O System (BIOS)

3.2.5 BOOT THE SYSTEM TRACK(S) FROM THE SELECTED DRIVE

Bytes 11-12H: DEFW BOOTER

On entry: DRIVE contains the selected drive

Action: the track-O of the selected drive is read to D600H. In case of error the "SYSTEM DISK?" message is displayed and the operator must depress any key except ESC to repeat.

If D603 = 80 a return is made

81 track-1 is read from the same side to E600H

82 track-0 is read from the other floppy side to $E600H_{\bullet}$

On exit: RWBUFF, RWLGT and all simple registers are destroyed.

3.2.6 GET LISTING DEVICE STATUS

Bytes 13-14H: DEFW LISTAT

Action: the USART control byte is read. DSR, TxRDY and TXEMPTY must be set for ready. (The printer READY BIT is connected to the USART DSR pin because it can be read directly from control byte.)

On exit: if device ready, A = FFH and zero flag is reset.

If device busy, A = 0 and zero flag is set.

All other registers are unchanged.

3.2.7 PRINT SCREEN

Bytes 21-22H: DEFW PRSCR

PRSCR is an auxiliary subroutine to print one or more lines from the screen.

On entry: BC = the screen address (top-left position is 0)

A =the number of lines to print (1 to 24)

On exit: A = FF and the zero flag is reset if printing successful

A = 0 and the zero flag is set if either:

- the range specified is out of the screen range

- a printer error has occurred

WARNING No key may be depressed during the print procedure.

Operating Systems Basic I/O System (BIOS)



3.3 System Timer

The system supports a 4 bytes long 60 Hz system timer. Its value can be accessed in DPB Bytes 29 to 2CH (29H is the lowest byte). This CLOCK field is cleared on reset unless the user depresses the SPACE bar.

The user can also define a subroutine that will be called in every $16.7~\rm ms$. Its address is stored at DPB bytes $25-26\rm H$. The user must save all registers and as no CP/M stack may be used a user defined stack must be set up.

3.4 Summary of the Driver Parameter Block

The pointer to this block is stored at FFDOH.

00	DRIVE	ACTUAL DRIVE NUMBER
	TRACK	
03	SECTOR	ACTUAL SECTOR NUMBER
04	HEAD	ACTUAL HEAD NUMBER
05	RWBUFF	READ-WRITE BUFFER ADDR
07	RWLGT	READ-WRITE LENGTH - 1
	RDS	READ SECT SUBROUTINE ADDR
OB	WRS	WRITE SECT SUBROUTINE ADDR
0D	STEP	SEEK SUBROUTINE ADDR IN PROM
OF	RECAL	RECALIBRATE SUBROUTINE ADDR IN PROM
11	BOOTER	BOOTER SUBROUTINE ADDR
13	LISTAT	LIST STATUS SUBROUTINE ADDR
		PRINT TABLE ADDR
17	PRWAIT	MAX PRINTER WAITING TIME IN 4 SEC UNITS
18	PRSTAT	PRINTER STATUS BYTE IS O IF PR ERR OCCURED
19	PRCONT	IF O, NO MESSAGE IF PRINTER NOT RDY
1A	BOOTDR	BOOTING DRIVE (0, FF OR 1)
1B	DSKFLG	INTERNAL DISK FLAG
1C	DMSTAT	DMA SHADOW BYTE
1 D	HDERSU	XEBEC ERROR ROUTINE ADDR FOR MAINTENANCE
1 F	DSKTR	00, C9 FOR STANDARD TRACK NUMBERING
		24, C9 FOR OLD PHILIPS TRACK NUMBERING
21	PRSCR	PRINT SCREEN SUBROUTINE ADDR
23	MSWBYT	O IF ROM, 2 IF RAM PROGR RUNS
24		C3 FOR JUMP
25	TINEX	ADDRESS OF EXTERNAL TIMER INT
27	KSTAT	KEY STATUS IS O IF NO KEY DEPRESSED
28	KBYTE	HOLDS THE LAST DEPRESSED KEY
29	CLOCK	4 BYTES LONG 60 HZ CLOCK
2 D	RESULT	7 BYTES LONG FIELD FOR FLOPPY RESULT BYTES





Operating Systems
Basic I/O System (BIOS)

3.5 Interrupt Vector Table

The interupt vector table has a fixed location: FFDOH. The CPU I register is always FF and it should not be changed!

CTC1 INTERRUPTS

FFD0	DEFW DRIVE	ADDRESS OF DRIVER PARAMETER BLOCK
FFD2	DEFW RETIN	
FFD4	DEFW RETIN	
FFD6	DEFW INTDMA	DMA INTERRUPT SUBROUTINE

CTC2 INTERRUPTS

FFD8	DEFW TIMER	TIMER INTERRUPT
FFDA	DEFW RETIN	
FFDC	DEFW RETIN	RESERVED FOR EXTENSIONS OR THE USER
FFDE	DEFW FDCINT	FLOPPY OR SASI INTERRUPT

SIO INTERRUPTS

FFEO DEFV	RETIN				
FFE2 DEFV	RETIN				
FFE4 DEFV	CONINT	CONSOLE			
FFE6 DEFV	CERINT	CONSOLE	ERROR	INTERRUPT	(OVERRUN)
FFE8 DEFV	RETIN				
FFEA DEF	/ RETIN				
FFEC DEF	RETIN				
FFEE DEF	V RETIN				

The range FFFO to FFFF is reserved for interrupts generated by any extension unit.

The address of any interrupt subroutine must be over 1000H.

If an extension card (e.g., IEC card) is implemented using the FFDC interrupt location, the user must not use it again.

Operating Systems Basic I/O System (BIOS)



CP/M INITIALIZATION

After a successful IPL procedure, control is transferred to the CP/M initialisation program. It is stored partly in the first 128 bytes of the IPL track, partly in the DIRBUF area that will be deleted later. A free space of about 30 bytes is reserved on the first IPL sector where the user can patch some special initializations; it is filled with HEX-0.

The CP/M initialization program has the following functions:

- modifies internal driver table and start up message if IPL has been done from floppy-2,
- fetches the addresses of CONST, CONIN, CONOUT, LIST1, PRSCR, COMOJP and COMIJP from the driver jumping table and patches them into the CBIOS
- fetches the addresses of subroutines from the driver parameter block and patches them into the CBIOS
- loads the keyboard table to the terminalboard
- loads the screen table to the terminalboard
- sends the CAPS LOCK properties to the terminalboard:
 - caps lock character is 80H
 - caps lock limit in ASCII table as configured CAPS LOCK is activated on startup if so configured.
- prints the startup message (PHILIPS P2000C .. K CP/M 2.2)

CP/M is shifted to the proper position, the CP/M jumps on the 0-page are set, and a jump is made to CP/M.

If a BASIC environment has been configured, no CP/M message is displayed, but the program BASIC.COM is loaded and started. The specified AUTOLOAD command is brought to the 80H...FFH range.

In the BASIC environment the CP/M cannot be used.

There is a special key in the CP/M implementation with the symbol σ . In the standard configuration its value is 80H and has a CAPS LOCK toggle function. If it is used together with the Supershift key, its value is 90H and it activates the PRINT SCREEN function.



Operating Systems Basic I/O System (BIOS)

3.5 Interrupt Vector Table

The interupt vector table has a fixed location: FFDOH. The CPU I register is always FF and it should not be changed!

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FFD0	DEFW DRIVE	ADDRESS OF DRIVER PARAMETER BLOCK
FFD2	DEFW RETIN	
FFD4	DEFW RETIN	
FFD6	DEFW INTDMA	DMA INTERRUPT SUBROUTINE

CTC2 INTERRUPTS

FFD8	DEFW TIMER	TIMER INTERRUPT
FFDA	DEFW RETIN	TOTAL TOTAL
FFDC		RESERVED FOR EXTENSIONS OR THE USER
FFDE	DEFW FDCINT	FLOPPY OR SASI INTERRUPT

SIO INTERRUPTS

FFEO	DEFW RETIN	
FFE2	DEFW RETIN	
FFE4	DEFW CONINT	CONSOLE INTERRUPT
FFE6	DEFW CERINT	CONSOLE ERROR INTERRUPT (OVERRUN)
FFE8	DEFW RETIN	
FFEA	DEFW RETIN	
FFEC	DEFW RETIN	
FFEE	DEFW RETIN	

The range FFFO to FFFF is reserved for interrupts generated by any extension unit.

The address of any interrupt subroutine must be over 1000H.

If an extension card (e.g., IEC card) is implemented using the FFDC interrupt location, the user must not use it again.

Operating Systems Basic I/O System (BIOS)



4 PERIPHERAL AND MEMORY DEBUGGER

4.1 General

If the BOOTER subroutine can not boot and the "SYSTEM DISK?" message is displayed, the user can type the ESC key to enter the debugger.

The primary aim of this module is to help troubleshooting. Even if booting is impossible it enables the user to make a short check for memory, ports, floppy disk, hard disk, video, keyboard and printer.

4.2 Commands

The debug program starts with the following prompt:

'Commands: C, D, DR, DW, F, G, M, P, PS, S, SK
Entry: Command Start_address, End_address, Other_info'

The command code may be followed by a space (not necessary). The separator between the operands may be a space or a comma. The syntax is similar to that of the DDT of Digital Research. An automatic caps lock function is implemented, i.e., lower case letters can not be entered.

To exit the debugger type 'GO (CR)' and any two characters (initial terminal handshake) or simply depress the reset

This section gives the commands that are implemented.

4.2.1 COMPARE MEMORY BLOCKS

button.

Example: C 4000 4FFF 5000

This command compares the block 4000 to 4FFF with 5000 to 5FFF and the differences are displayed.



Operating Systems Basic I/O System (BIOS)

4.2.2 DISPLAY MEMORY BLOCK

Example: D 6000 607F

The contents of the range 6000 to 607F is displayed (hex and ASCII). As the program stores the last displayed address and the length of block, the user has only to enter D and RETURN to see the next block (6080 to 60FF). The first D and RETURN entry shows the range 4000 40FF. (4000 is the first address of the default disk buffer). After a disk read or write command the actual disk buffer address overwrites this address. A long display may be stopped temporarily by the CTRL-S character. After the next CTRL-S it is continued, any other character cancels the command.

4.2.3 DISK READ TRACK

Example: DR 126 5000

Reads drive-1 track 26 (decimal) to 5000 through 5FFF.

The first digit is the drive number:

1: Floppy-1 first side

2: Floppy-2 first side

3: Floppy-3 first side

4: Floppy-4 first side

5: Floppy-1 second side

6: Floppy-2 second side

7: Floppy-3 second side

8: Floppy-4 second side

9: Hard disk-1

The second and third digits give the track number. For floppies it must be 0 to 79, for hard disk 0 to 99 (i.e., only a small part of the hard disk can be read this way).

If no read address is given, the default value is 4000.

The defined track is read continuously until any key is depressed and the result of each 'read' is displayed. The result will be either OK or, in the event of an error, the RESULT bytes of the uPD765 Floppy controller. (In the case of hard disk error this RESULT byte has no meaning).

Operating Systems Basic I/O System (BIOS)



4.2.4 DISK WRITE TRACK

Example: DW 69

The data from 4000 to 4FFF is written to drive-2, second side, track-9. ALL characteristics given for the read function are valid here too.

4.2.5 FILL THE MEMORY BLOCK WITH ONE BYTE

Example: F 8233 875D 55

The range 8233 to 875D is filled with 55H.

4.2.6 GO TO AN ADDRESS (CALL A PROGRAM)

Example: G 5000

The user can enter small programs with the S(et) command and execute with G. The C9 (RET) instruction leads back to the debugger.

4.2.7 MOVE MEMORY BLOCK

Example: M 4000 4FFF 5000

The block 4000...4FFF is copied to 5000...5FFF.

4.2.8 PORT READ/WRITE

Example: P 2A

The port address 2A is read, after which the user can enter a byte that is output to the port. Afterwards port 2B can be read...and so on. If nothing has to be output, type RETURN. To cancel the command type '.' and RETURN.

The command P and RETURN displays the port map 00..FF.



Operating Systems
Basic I/O System (BIOS)

4.2.9 PRINTER SWITCH

Example: PS

After entering the PS command all information on the monitor is printed. It can be cancelled by another PS command.

4.2.10 SET MEMORY

Example: S 4000

The first address and its contents will be displayed.

4000 21 - original contents 21H

The contents can be altered [enter new value], or left unchanged [enter CARRIAGE RETURN]. The next address will then be displayed. To cancel the command, enter '.'

- changes contents to 31H 4000 21 31 - changes contents to 10H 4001 00 - leaves contents as 50H 4002 50 - changes contents to 3AH 4003 32 3A 4004 - cancels command 55

Invalid inputs (outside the range 0 - 9, A - F) will be treated as zeros.

4.2.11 SEEK STRING IN MEMORY

Example: SK CD F9 F6

All addresses where the string CD F9 F6 occurs are displayed.

Operating Systems Basic I/O System (BIOS)



5 CP/M INITIALIZATION

After a successful IPL procedure, control is transferred to the CP/M initialisation program. It is stored partly in the first 128 bytes of the IPL track, partly in the DIRBUF area that will be deleted later. A free space of about 30 bytes is reserved on the first IPL sector where the user can patch some special initializations; it is filled with HEX-0.

The CP/M initialization program has the following functions:

- modifies internal driver table and start up message if IPL has been done from floppy-2,
- fetches the addresses of CONST, CONIN, CONOUT, LIST1, PRSCR, COMOJP and COMIJP from the driver jumping table and patches them into the CBIOS
- fetches the addresses of subroutines from the driver parameter block and patches them into the CBIOS
- loads the keyboard table to the terminalboard
- loads the screen table to the terminalboard
- sends the CAPS LOCK properties to the terminalboard:
 - caps lock character is 80H
 - caps lock limit in ASCII table as configured CAPS LOCK is activated on startup if so configured.
- prints the startup message (PHILIPS P2000C .. K CP/M 2.2)

CP/M is shifted to the proper position, the CP/M jumps on the 0-page are set, and a jump is made to CP/M.

If a BASIC environment has been configured, no CP/M message is displayed, but the program BASIC.COM is loaded and started. The specified AUTOLOAD command is brought to the 80H...FFH range.

In the BASIC environment the CP/M cannot be used.

There is a special key in the CP/M implementation with the symbol σ . In the standard configuration its value is 80H and has a CAPS LOCK toggle function. If it is used together with the Supershift key, its value is 90H and it activates the PRINT SCREEN function.





Operating Systems Terminal Board Firmware

1 GENERAL

1.1 Memory Layout

```
-I-
FFFFH
                                  Character mode attribute RAM
          I ▼···E800H - FFFFH
E000H
         -I-
          Ι
DOOOH
         -I-
          Ι
                                16 kB attribute & graphic RAM
         -I- ♦...COOOH - FFFFH
C000H
                                  2 kB Character video RAM
          I ◄...B800H − BFFFH
         -I- v···Program stack
                                  (starting at B800H)
B000H
          Ι
H000A
         -I-
          Ι
9000H
         -I-
          I ...RAM FREE TO USE (returned by STATUS info.)
         -I- <...Start of program RAM area (tables & variables)
H0008
7000H
6000H
5000H
                 ADDRESSING SPACE FOR 2 X 16 kB ROM
4000H
3000H
2000H
         -I-
          Ι
                                   8 kB ROM (PROGRAM)
1000H
         -I-
                 0000H - 1FFFH
          Ι
0000H
```

The RAM area from RAM FREE TO USE to (B800H - STACK) may be used by the user-program (loaded in INTEL-HEX FORMAT). The area from COOOH to E800H may also be used if the High Resolution Graphic mode is not used. The RAM FREE TO USE is fixed for any particular software release but may change on re-issue.

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1.2 Features

1.2.1 COMMUNICATION

Asynchronous up to 19200 Bd. (Queued in both directions in a 255 byte queue.)

1.2.2 KEYBOARD

8-bit code supporting national versions. Standard ASCII key table in ROM, download of national versions possible. Keys queued.

1.2.3 SCREEN

8-bit code (national versions) 24 lines/80 characters

Character Mode

- Bidirectional scrolling
- Split-screen capability (partial scroll)
- Three Attribute modes:

Manual Read and write data from/to attribute page

(normal memory access).

Auto duplicate: The read attribute data will be duplicated.

Block mode: For "block

For "block moves" such as scrolling, the attribute page will be scrolled

automatically.

- Attributes: Underline)

Invert) and all

Blink) combinations

4 Intensity levels)

- Adjustable TABs
- Teletext graphics
- Text and Attributes back-transfer from screen possible.



Operating Systems Terminal Board Firmware

High Resolution Graphics Mode

- 2 selectable modes
512 x 252 dots (no attributes)
256 x 252 dots (3 intensity levels + background)

Each dot addressable Simple vector handling:

- In Cartesian and Polar co-ordinates.
- Combination with character mode (characters: 21 lines/64 characters).

2 DETAILED DESCRIPTION

2.1 Communication

The communications control between the terminal and the CPU is done by the V24 control lines. Transfer rate is asynchronous at 19200 Baud.

2.1.1 Transfer - CPU to Terminal

Note: RTS of terminal is connected to CTS of CPU and CTS of of terminal is connected to DTR of CPU.

The terminal sets RTS (data terminal ready) if it is ready to receive. (Normal situation)

The CPU can send data, but has to check if CTS is high during sending (this is done by hardware).

The terminal stores the characters in an internal queue and resets RTS when the queue is full or the terminal is no longer ready to receive.

2.1 2 Transfer - Terminal to CPU

This is done the same way.

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2.2 Keyboard

The pressed keys will be converted into the extended ASCII-code corresponding to the key tables and stored in a queue. If there is a character in the queue the terminal will send it to the CPU as described.

2.3 Screen and Screen Codes

The screen is controlled by both single codes and ESCape sequences.

2.3.1 SINGLE CODES

The single codes are shown in the following table:

ACTION	Code	2
Cursor Home	SOH	01H
Cursor Forward	ACK	06H
Cursor Down	LF	OAH
Cursor Up	SUB	1AH
Cursor Back	NAK	15H
Bell-Beep	\mathtt{BEL}	07H
Backspace	BS	180
TAB	TAB	09Н
Clear Screen	FF	OCH
CR	CR	ODH
End of Page (column 80, row 24)	EOT	04H
Reset Terminal	CAN	18H
CAPS LOCK	SI	OFH
Lock Keyboard	EM	19H
Unlock Keyboard	STX	02H

Note: The Reset Terminal command (18H) causes a software reset (re-initialize) to the terminal software. It has the following effects:

- Clears receive and transmit queues
- Resets TABS to every 8 columns
- Clears the screen
- Unlocks all locked areas

After the RESET command the terminal is unable to receive characters for about 200 $\ensuremath{\mathsf{msecs}}_{\:\raisebox{3.5pt}{\text{\circle*{1.5}}}}$



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CONTROL CODE (CTRL) GENERATION

Any code between 00H and 1FH, received by the Terminalboard, is treated as a CONTROL character and is used to initiate special actions. These are shown, as Single Codes, in the table on the previous page. It should be noted that the mnemonics given to these codes are of a general (Data Communications) nature, and do not always reflect their use within the P2000C. For example, the codes 01H (SOH - start of heading) and 06H (ACK - acknowledge) have no relation to the cursor movements produced by these codes in the P2000C. On the other hand the code 08H (BS - backspace) is used for that function.

To warn the Terminalboard that a CONTROL character will be sent, the CTRL key must first be pressed. This will be indicated on the Monitor with the symbol "^". The hexadecimal code of the following key will then be treated as the CONTROL character. The second character of the control code will always be taken from columns 4 and 5 of the ASCII table. See table below.

Generally, the character following the CTRL will come from the main ASCII character set, in the range 20H to 7FH. This value will be reduced by 60H, 40H or 20H; to give a value between 00H and 1FH.

As the P2000C only uses the least significant 7 bits of a generated character code, a code between AOH and FFH will be reduced by 80H, the resultant value, in the range 20H to 7FH, being treated as above.

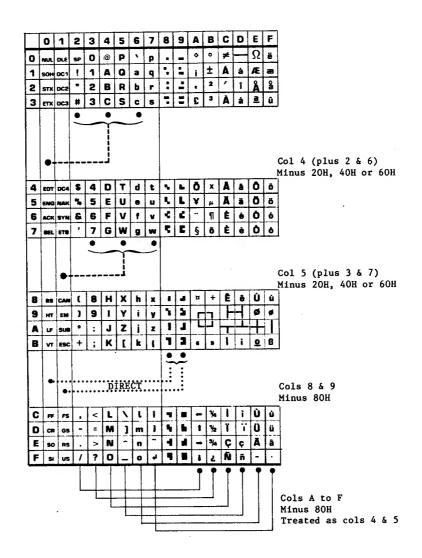
Direct CONTROL characters can be produced by setting the Keyboard Table to produce codes in the range 00H to 1FH. In this case the CTRL key would not be used. Similarly, if a value between 80H and 9FH is produced, via the Keyboard Table, the reduction by 80H will also give direct CONTROL characters.

CTRL	ACTION	CODE	CTRL	ACTION	Code
^A ^J ^U ^H ^L	Cursor Home Cursor Down Cursor Back Backspace Clear Screen	01H 0AH 10 15H 21 08H 0CH 12	^F ^Z ^G ^I ^M	Cursor Forward Cursor Up Bell-Beep TAB CR	06H 1AH 26 07H 09H 0DH 13
^D ^O ^B	End of Page (col 80, row 24) CAPS-LOCK Unlock Keyboard	04H 0FH *5 02H	^X ^Y	Reset Terminal Lock Keyboard	18H 24 19H 25

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In the following diagram the standard ASCII table is annotated to show the effect of using the CTRL key with any key-produced code. For example, the codes associated with any of the keys '7', 'W' or 'w' (37, 57 or 77) would produce the CONTROL code '17' (ETB), which is not used in the P2000C Basic I/O System.





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2.3.2. ESCAPE SEQUENCES - SET ATTRIBUTE

SET ATTRIBUTE = ESC,0,b

where b=attribute byte and 0=numeric zero

An attribute can be set at any time and is valid until a new attribute is selected.

Attributes: Underline - UL

Blink - BL Invert - INV 4 Intensities

res - reserved

Attribute byte: |res|inl| UL|INV|res|res| BL|in2| |---|---|---|---| **4 3** දු 5 bit: Ð | inl | in2 | Intensities Quarter bright | 0 | 0 | 1 | Bold 1 | 0 | Normal Half bright 1 1

For example, the ESCape sequence ESC,0,99 (or ESC,0,&H63) would cause screen characters to be produced:

- half brightness
- underlined
- blinking

Note: To execute ESCape sequences it is necessary to use the CHR\$(27) code.

All ESCape sequences in the following pages can be carried out in this way. The above example could be included in a BASIC program in the following way:

PRINT CHR\$(27)+"0"+CHR\$(&H63)

or

PRINT CHR\$(27)+"0"+CHR\$(99)

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2.3.3 ESCAPE SEQUENCES - SCREEN CONTROL

ACTION		Code	ASCII
Cumpan Addmonaina		ESC,Y,r,c	V-50H/80
Cursor Addressing $r = row$	- 0 t	o 23 (+20H offse	
		o 79 (+20H offse	
	иши — О С		K=4BH/75
Erase to End of Line		ESC,K	k=6BH/107
Erase to End of Screen		ESC,k	S=53H/83
Scroll Up one Line		ESC,S	
Scroll Down one Line	•	ESC,T	T=54H/84
Set TAB at Cursor Posit		ESC,I	I=49H/73
Clear TAB at Cursor Pos	sition	ESC,G	G=47H/71
Clear all TABs		ESC,g	g=67H/103
Insert Line		ESC,L	L=4CH/76
Delete Line		ESC,1	1=6CH/108
Insert Character at			
Cursor Position	ON	ESC,Q	Q=51H/81
	OFF	ESC,R	R=52H/82
Delete Character at			
Cursor Position		ESC,P	P=50H/80
Insert Character			
Wrap-around	ON	ESC, N	N=4EH/78
•	OFF	ESC,R	R=52H/82
Delete Character		•	·
Wrap-around		ESC,O	0=4FH/79
Back TAB		ESC,i	i=69H/105
Cursor Visible		ESC,C	C=43H/67
Cursor Invisible		ESC,c	c=63H/99
			1=31H/49
Start Teletext Graphic		ESC,1	1=31H/49 2=32H/50
End Teletext Graphic	_	ESC,2	-
Lock Area for Scrolling		ESC,A,n	A=41H/65
** 1 1 A C		er of lines	(111/07
Unlock Area from curso	r	ESC,a	a=61H/97
Unlock all Areas		ESC, u	u=75H/117
Send Status		ESC,?	?=3FH/63
Send Text from Cursor			\$=24H/36
		ber of character	:s
Send Attributes of Text	t		
from Cursor		ESC,%,nn	%=25H/37
Load User Program		ESC,p	p=70H/112
(in INTEL HEX for	nat)		
End of INTEL HEX Format	•	ESC,:	:=3AH/58
(exits loader, no			
Execute User Program		ESC,x	x=78H/120
Load New Keyboard Table	e	ESC,@	0=40H/64
	-	, -	
		ESC.!	!=21H/33
Load New Screen Table Define Caps Lock Key		ESC,! ESC,+,k,nn	!=21H/33 +=2BH/43



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2.3.4 DESCRIPTION OF CONTROL CODES

Cursor home: New cursor position is column 1/row 1.

Cursor forward: Column + 1.

Cursor down: New line. Scroll if last line or beginning of

a locked area.

Cursor up: One line up. If 1st line then new position is

the bottom line.

Cursor back: Column - 1.

Backspace: Same as cursor back.

TAB: Cursor to next TAB position, default every

eighth column.

Clear screen: Erase the whole screen, cursor at home

position.

CR: Cursor at column 1 in current line.

End of page: New cursor position is column 80 and row 24 Reset terminal: Initialise hardware and software. After RESET

allow 500ms before sending data to terminal.

Lock keyboard: All keyboard inputs are ignored. Unlock keyboard: Keyboard entries are re-enabled.

Reset: Re-initializes the hardware and software.

Set attribute: A new attribute is used until the next "Set

attribute" command.

Cursor address: Absolute cursor address with an offset of 20H

(ESC, Y, 20H, 20H is the "home position").

Erase to end Clear all characters including cursor position

of line: to column 80.

Erase to end Same as "Erase to end of line" to column 80,

of screen: row 24.

Scroll up 1 Scroll up the whole screen or area and clear

line last line.

Scroll down 1 Same as above, but scroll down.

line

Set TAB: Sets a new TAB position at cursor position.
Clear TAB: A TAB position is removed at cursor position.

Clear all TABs: Removes all TABs.

Insert line: Scroll down the lines from cursor line + 1,

and clear cursor line.

Delete line: Scroll up the lines from cursor line +1 to

cursor line.

Insert ON: The next character will be inserted at cursor

position, the last character in the line will

be lost.

Insert wrap- Same as "Insert" but the last character of the

around: screen will be lost.

Insert OFF: Exit insert mode, normal overwrite.

Delete Delete character at cursor position, the last

character: character in the line will be a blank.

Delete Same as "Delete character" but last character

character wrap of screen will be blank.

around:

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Back TAB: New cursor position is previous TAB position.

Cursor visible: Display cursor.

Cursor invisible:Do not display cursor.

Start Teletext All characters between 20H & 3FH, and 60H

graphic:

& 7FH are interpreted as teletext characters.

End Teletext Normal character mode.

graphic:

Lock area: From cursor line, n lines will be locked.

(This area will not be scrolled by Cursor up and down, only by explicit "Scroll up (down)" command. (See Scroll Lock explanation on

following pages).

Unlock area: The cursor position area is unlocked.

Unlock all: Normal screen status.

Send status: 12 bytes terminal status information will be

sent (see STATUS INFORMATION).

Send text: nn characters from cursor position will be

sent back.

Send attribute: nn attribute bytes from cursor position will

be sent.

Load user PGM: This function enters a built in INTEL-HEX

FORMAT loader. The load address may be anywhere in the free RAM areas (see Memory layout). To find RAM FREE TO USE use the

STATUS command (ESC,'?').

The terminal remains in the LOADER until it recognises an ESC,':' after a valid INTEL_HEX FORMAT record. If loading is finished, normal

terminal operation is possible.

End loader: Exits the loader, enables normal operation.

Execute PGM: This function makes a CALL to the previously

loaded user program. The user program entry address is defined by an INTEL_HEX_FORMAT record with record-type '01'. Ensure that the loaded program has such a record, otherwise a CALL to the location '0' will be performed (RESET). Only the last '01' record is valid. The user program should exit via a 'RET'

The user program should exit via a KEI instruction, making a normal return to the

terminal program.

Load new Loads the following 360 bytes into the

keyboard table: internal keyboard table. It consists of 4 90

byte sub-tables (NORMAL, SHIFT, SUPER SHIFT, SUPER SHIFT-SHIFT) (see STANDARD KEY TABLE).

Note: If CONTROL is pressed, all key codes

are logically ANDed with 1F.

Load new screen Loads the following 256 bytes into the

table: internal screen table.

Define Caps Lock The key K is the new caps lock key. There is

key: no default key.





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SCROLL LOCKED AREAS

Normally, all 24 lines of the screen will be scrolled by a LINE FEED on the last line or by an explicit SCROLL UP - SCROLL DOWN command. For some applications it is useful not to scroll the whole screen e.g., in word processing (tab - format line). On the P2000C it is possible to lock certain areas of the screen, or the whole screen, from automatic scrolling. This is done with the command ESC, 'A', n. It locks n lines, starting with the cursor line. Normal scrolling is still possible with the explicit SCROLL UP - SCROLL DOWN commands.

EXAMPLES

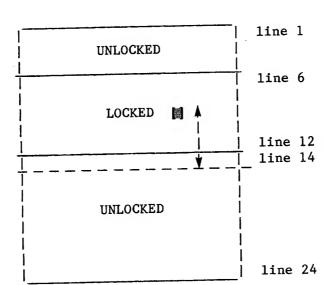
	line 1
	line 6 = cursor line
	line 12
	Sending the sequence: 1BH, 41H, 7H will lock lines 6 to 12 from scrolling
	line 24

UNLOCKED		Scrolling will occur in this area when reaching line 5 (lines 1 - 5 only)
LOCKED	line 6	Writing in this area will cause overwriting when line 12 is reached as the area is locked
UNLOCKED	True 1	Scrolling will occur in this area (lines 13 - 24 only) when reaching line 24
	line 2	Use cursor addressing command ESC,'Y',r,c to 4 leave locked area.

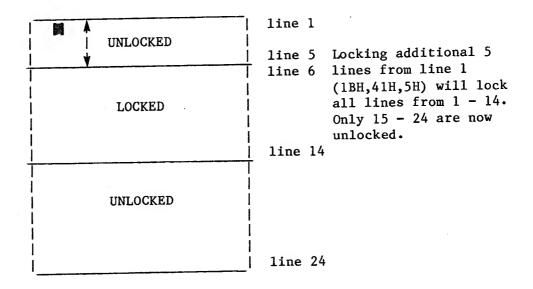
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ALLOCATING MORE SCROLL LOCKED LINES



If sequence 1BH,41H,5H with cursor in line 10, the lines 10 - 14 will be locked. As lines 10, 11 and 12 are already locked, the locked area will simply be increased







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LAST PART OF THE SCREEN IS LOCKED

UNLOCKED	line l	
UNLOCKED	line 5	
LOCKED		If the cursor is any- where in the locked area at bottom of the screen,
	line 10	writing in bottom
		line will cause the cursor to move to the top of the screen. The same effect is seen when
	line 17	the whole screen is
LOCKED		locked.
	line 24	

The UNLOCK command will unlock the complete area containing the cursor. If the cursor is in an unlocked position when the command is given it has no effect.

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2.3.5 GRAPHIC CONTROL

ACTION	Code	ASCII
Start high resolution mode 1		- 0577/50
(256×252)	ESC,5	5=35H/53
Start high resolution mode 2	B00 3	3=33H/51
(512×252)	ESC,3	333π/ JI
Start character mode	ESC,4	4=34H/52
(end graphics)	150,4	4 3411, 32
CARTESIAN CO-ORDINATES:		
Clear dot	ESC,d,xy	d=64H/100
Set dot	ESC, D, xy	D=44H/68
Move to	ESC,m,xy	m=6DH/109
Draw to	ESC,M,xy	M=4DH/77
Clear to	ESC, v, xy	v=76H/118
POLAR CO-ORDINATES:		
Set origin	ESC,z,xy	z=7AH/122
Move to	ESC, y, Aabs	y=79H/121
Draw to	ESC, U, Aabs	U=55H/85
Clear to	ESC, w, Aabs	w=77H/119
Set dot	ESC,F,Aabs	F=46H/70
Clear dot	ESC,f,Aabs	f=66H/102
Send picture (to screen)	ESC,r,xy,nn	r=72H/114
	er of bytes	
Receive picture (main processor)	ESC,t,xy,nn	t=74H/116
Note: xy = co-ordinates: 2	bytes in mode 1	
	bytes in mode 2	
(low 'x' byte first, i.e., x(low), x(high), y		
Aabs = A + abs:		
A = angle ALPHA (2 bytes)		
abs = absolute va		

In commands, Aabs parameters (4 bytes) are as follows:

byte 1 = A MOD 256 byte 2 = INT(A/256) byte 3 = abs MOD 256 byte 4 = INT(abs/256)

It should be noted that any movement of data from the screen as in, e.g., Send/Receive Picture, Get Status commands etc., may result in the generation of code 90H. This could be interpreted by the Terminalboard as a Print Screen command. It is advisable to disable the Print Screen function where this could be inconvenient.



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Angle ALPHA "A" is in steps of one degree (0 to 360).

Defining angle "A"; 2 bytes (low order byte FIRST in command)

low order byte: = A MOD 256

high order byte: = INT(A/256)

Defining value "abs"; 2 bytes (low order part FIRST in command)

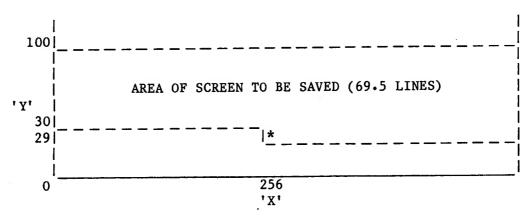
low order byte: = abs MOD 256

high order byte: = INT(abs/256)

DESCRIPTION OF SEND/RECEIVE PICTURE

In either of the high resolution graphics modes, an area of the screen can be stored for rapid retrieval by using the ESC r & t sequences.

The sequence ESC,t,xy,nn (defined as Receive Picture - the main processor 'receives' the information) defines the first co-ordinate of the screen image to be stored (xy) and the number of bytes to be stored (nn). Remember that in the 512 X 252 resolution mode the 'x' co-ordinate requires 2 bytes. The number of bytes must be calculated at 64 bytes for each complete line to be stored. The first byte to be stored is calculated from the xy co-ordinates, rounded down to ensure that the full picture is stored.



ESC, 't', 0 ,1 ,29, (69.5 x 64) x1 ,x2 ,y , n1 , n2 1BH, 74H, 0 ,1 ,29, 96 , 17

The sequence ESC,r,xy,nn (defined as Send Picture - the main processor 'sends' the information to the terminal) defines the start position of the picture on the receiving screen (xy) and the number of bytes to be transferred (nn).

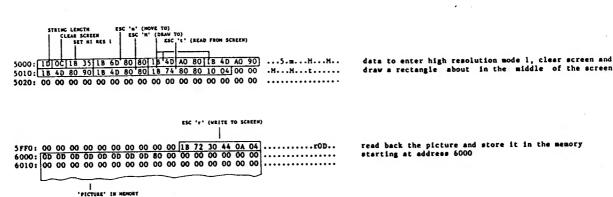
ESC, 'r', 0 ,1 ,29, (69.5 x 64) x1 ,x2 ,y , n1 , n2 1BH, 72H, 0 ,1 ,29, 96 , 17

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EXAMPLE PROGRAM SHOWING SEND/RECEIVE PICTURE USING ZSID

```
4000 LD
           HL,5000
                    nr. of bytes to be printed (stored at 5000H)
4003
     LD
           B,(HL)
     INC HL
4004
     LD C,(HL)
PUSH BC
                     get next data byte
4005 LD
                     save register
4006
4007
      PUSH HL
                     save register
4008
      CALL F60C
                     print (on console)
     POP HL
POP BC
400B
                     restore register
400C
                     restore register
400D
      DJNZ F5 (4004)loop for all bytes to be printed
400F
      NOP
4010
      NOP
4011
           C,04
                     number of bytes to read back from screen (410hex)
      LD
4013
      LD
           B,10
                     write bytes from screen to memory starting at address 6000
4015
      LD
           HL,6000
4018
      PUSH BC
                     save register
      PUSH HL
                     save register
4019
401A
      CALL F609
                     get one byte from screen
                     restore register
401D
     POP HL
      POP BC
                     restore register
401E
           (HL),A
                     save byte from screen to next free location
401F
      LD
      INC HL
                     move to next location
4020
               (4018)loop for all bytes requested
4021
      DNJZ F5
      LD,
DEC
           B,FF
                     next 256 bytes
4023
                     until register C contains 0
          C
4025
           A,C
4026
      L.D
4027
      CP
           FF
           NZ,ED (4018)
4029
      JR
      NOP
402R
402C
      NOP
402D
      NOP
402E
      NOP
402F
      NOP
4030
      NOP
           C,04
                     nr. of bytes to be printed (416hex)
4031
      LD
4033
      LD
           B,16
                     start printing bytes at address 5FFA
4035
      LD
           HL,5FFA
      PUSH HI.
4038
                      save register
4039
      PUSH BC
                      save register
                      print byte, addressed by register HL
           C,(HL)
403A
      LD
      CALL FOOC
403B
      POP BC
403E
                      restore register
      POP
           HL
403F
                      restore register
                      move to next location until all characters are printed
4040 INC HL
               (4038)
4041
      DJNZ F5
           B,FF
4043 LD B,
4045 DEC C
           A,C
4046 LD
4047
      CP
           FF
4049
      JR
           NZ,ED
404B
                      stop program here (set a breakpoint, or execute a return)
```





2.3.6

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DESCRIPTION OF GRAPHIC COMMANDS

252 resolution mode with 3 Start mode 1: Start 256 X

intensity levels. The change of this level is

done by "Set attribute" command.

Start mode 2: Start the 512 x 252 resolution mode.

Start character

mode: Exit high resolution graphic mode 1 or 2.

CARTESIAN COORDINATES

Erase pixel at screen position xy. Clear dot:

Set a pixel at xy. Set dot:

Move to: Set the internal cursor field to xy.

Draw a line from internal cursor field to xy, Draw to:

and set the internal cursor field to xy.

Same as "Draw to" but the line is erased. Clear to:

POLAR COORDINATES

Set the internal origin field to xy. Set origin:

Erase a pixel at A (angle), abs (absolute Clear dot:

value) with respect to the origin.

Same, but set the pixel. Set dot:

Set the internal cursor field to the calculated Move to:

(using A abs, origin) value xy.

Draw a line to the calculated value xy and set Draw to:

internal cursor field to xy.

Note: Any combination of POLAR and CARTESIAN coordinates is

possible!

"Start" command the graphic screen is cleared After a (but not the character part), the internal cursor field

and the origin field are set to 0.

On the following page is an example of a simple Basic program using polar co-ordinates in High Resolution Mode 2. This shows the use of some of the Graphic Control ESCAPE sequences given in 2.3.5. A more sophisticated example of the program is given in Appendix B of the manual.

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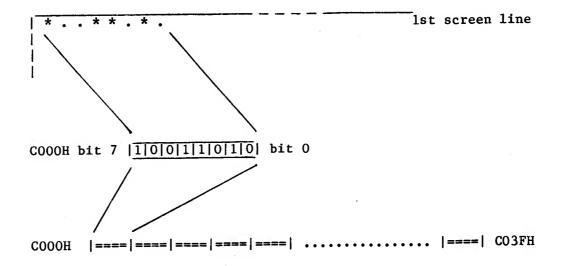
2.3.7 EXAMPLE - BASIC PROGRAM USING POLAR CO-ORDINATES

```
1 'simple test program for polar co-ordinates 2 '-----
10 DEFSTR E:ESC=CHR$(27):PRINT CHR$(12)
11 PRINT ESC"c
                                                      cursor invisible
                                                      'high resolution mode 2
12 PRINT ESC"3"
                                                      'set origin polar
13 PRINT ESC"z"CHR$(0)CHR$(1)CHR$(126)
14 PRINT ESC"y"CHR$(0)CHR$(0)CHR$(0)CHR$(0)
15 V=V+15:IF V==126 THEN 27
                                                      'move to origin
                                                      'setting of value V
                                                      '2 byte calculation of value
16 V1=INT(V/256):V2=V MOD 256
                                                      'setting of step rate
18 IF F=0 THEN S=14 ELSE S=45
                                                      'start loop in degrees
19 FOR A=0 TO 360 STEP S
                                                      '2 byte calculation of angle
20 A1=INT(A/256):A2=A MOD 256
                                                      'draw to command
21 PRINT ESC"U"CHR$(A2)CHR$(A1)CHR$(V2)CHR$(V1)
22 IF F=1 THEN 24
23 PRINT ESC"y"CHR$(0)CHR$(0)CHR$(0)CHR$(0)
                                                      'move to origin
24 IF F=0 THEN 25 ELSE FOR T=1 TO 50:NEXT T
                                                      'end of loop
25 NEXT A:GOTO 13
26
27 IF F=1 THEN 28 ELSE F=1:V=5:GOTO 12
28 F=0:V=5:GOTO 12
```

2.3.8 Description of Graphic RAM

512 X 252 MODE

In this mode, 1 byte represents 8 pixels, each pixel consisting of ONE screen dot. When a bit is ON (1) the corresponding pixel is visible. The msb (most significant bit) of each byte relates to the leftmost screen pixel. The first 64 bytes of graphic RAM (COOOH to CO3FH) represent the first (top) line of the screen, 64 x 8 giving the 512 pixels in each line.



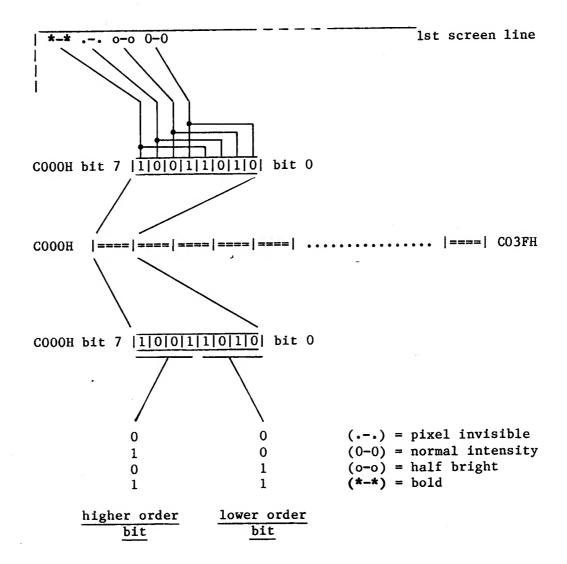




Operating Systems Terminal Board Firmware

256 X 252 MODE

In this mode, I byte represents 4 pixels, each pixel consisting of TWO adjacent screen dots. The first 64 bytes of graphic RAM (COOOH to CO3FH) represent the first (top) line of the screen, 64 x 4 giving the 256 pixels in each line. Each pixel is defined by 2 bits, with the msb (most significant bit) and msb minus 4 relating to the leftmost screen pixel. The values of these two bits determine the pixel intensity, i.e.,



Operating Systems Terminal Board Firmware



2.4 Status Information

The terminal status information is given in the form of a 12 byte string, as shown below:

Byte		Contents	
Number			
1		cursor position - column	
2		cursor position - row	
3		character at cursor position	
4		status flag	
	Bit:		
	0	1 = graphics on	
	1	1 = graphic mode 2	
		1 = teletext on	
	2 3	1 = insert mode on	
	4	<pre>1 = insert wrap around on</pre>	
	5	<pre>1 = keyboard is locked</pre>	
	6	reserved	
	7	reserved	
		internal graphic cursor field	
5,6		x co-ordinate	
7		y co-ordinate	
8,9		free space pointer (beginning of RAM area for user program)	
10,1	1,12	reserved for future use	



1

Hardware Configuration and Peripheral Extensions

HARDWARE CONFIGURATION

This chapter describes the Philips P2000C system hardware configuration. (For a description of the peripherals consult the appropriate peripheral reference manual). This chapter includes a description of the mechanical construction, electronic design, environmental conditions for storage and operation and power supplies.

1.1 INSTALLATION

After unpacking the basic P2000C, installation is simply a matter of connecting the keyboard to the main unit and then connecting the system to a suitable power supply. It should be confirmed that the voltage and frequency of the supply meets the requirements of system and any peripheral units that are to be connected. With the exception of the keyboard, all parts of the system are internally connected. Any additional units will be connected to the rear of the main unit by cables.

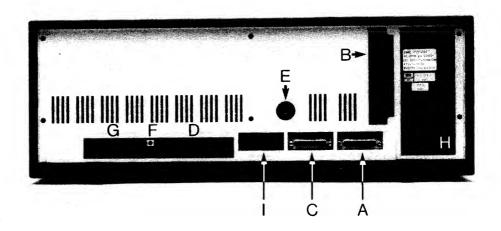


Figure 1.1 P2000C Rear Panel

Explanation of lettered items:

- A Printer connection B Position of extension
- C Communications connection (i.e., IEEE) connector
- D Hard disk connection E External video output
 - F Common earth for peripherals
 - G Connection to the external disk drives
 - H Mains power supply (inside compartment)
 - I Position of external terminal connection

Hardware Configuration and Peripheral Extensions



1.1.1 Connecting The Mains Supply

The P2000C contains an integral power unit. A cable is provided to connect the power supply to a suitable mains outlet. The keyboard is provided with power from the main unit via the connecting cable. Separate mains cables will be required for any peripherals (printer etc.). Mains cables are provided appropriate to the local conditions.

As soon as power is applied, by pressing the POWER ON/OFF switch, the system performs the IPL program and attempts to bootload the system software from a system disk. Failure to find suitable information (i.e., disk drive open) will result in a 'SYSTEM DISK?' message. Pressing the RESET switch on the front of the unit, or any key, will cause the IPL operation to be repeated.

1.1.2 Earthing

It is essential for safe operation that all components are connected to an earthed mains supply. Also, to remove the risk of errors caused by different earth potentials, all system hardware components must have a common ground. Two ground connections are provided on the rear panel for use of the printer or other peripherals.

1.1.3 Adjustment of Power Supply

Your P2000C will be set to the correct voltage for your district at manufacture. If it is necessary to alter the voltage, please refer to Part 3, Chapter 1.





Hardware Configuration and Peripheral Extensions

1.1.4 Optional Extensions

An important feature of the P2000C is the extension capability of the basic unit. It is possible to add either:

- IEEE Board
- RAM-Floppy Board

The procedure for fitting these boards is detailed in Part 4 of this manual and should be followed carefully.

1.2 MECHANICAL CONSTRUCTION

The P2000C is a portable desk-top microcomputer. It consists of a main cabinet containing monitor and disk drives with a keyboard attached by a cable to the side of the basic unit. Other system components that may be attached to the unit include additional disk drives, a printer and a second monitor.

Hardware Configuration and Peripheral Extensions



1.2.1 Dimensions of System Components

P2000C (including keyboard)

width 540mm
depth 360mm
height 210mm
weight 15.4 kg

1.2.2 Cable Specifications and Lengths

Mains power lead (including moulded plug)

length

1.8 metres

type

earthed mains lead

no. of cores

3

Main unit to Keyboard

1ength

1.3 metres

type

6-pole DIN 45 322 (240°)

no. of cores

6 + screen



Hardware Configuration and Peripheral Extensions

1.3 SAFETY

The P2000C is a Class I equipment and meets the following safety standards:

- IEC Publication 435, Draft 1983
 - Safety of data processing equipment
- OVE-EM 42 part 1, dated 1970 & part 2(1600)dated 1974
 - Requirements for electrically energised equipment for domestic use and similar purposes.
 - part 1/1970 General requirements - part 2(1600)/1974 Office machines

Hardware Configuration and Peripheral Extensions



1.4 ENVIRONMENTAL CONDITIONS

The environmental constraints imposed on the Philips P2000C microcomputer are in line with those for Philips office equipment, and should allow the equipment to function in a standard office environment as specified in Data Systems Environmental Standard, anywhere in the world without modification. If local operating conditions are outside these limits, then the local Philips service organization should be contacted. In addition, local office safety regulations may affect equipment operation, e.g., a limit on the time a user can continuously operate with a monitor.

1.4.1 Conditions for Storage of Components

The storage temperature and humidity figures for the individual system components are given in table 1.1. These figures assume that the combined rate of temperature and humidity changes preclude condensation on any part of the unit or media. Air transport under unpressurised conditions can take place at altitudes of up to 6300 metres.

1.4.2 Transportation Constraints

When packed for shipment the system components will suffer no degradation in performance when subject to shock and vibration in the x, y and z axis (within the limits set out below).

- continuous vibration (i.a.w. IEC 68)
 - 10 through 58 Hz maximum 0.3 mm amplitude (peak-to-peak)
 - 58 through 150 Hz maximum acceleration or deacceleration of 19.62 m/sec² (2g) in 3 axes, 1.5 hr/axis sweep 1 octave per minute.
- intermittent shocks
 up to 49.15 m/sec². (5g)

and not exceeding 11 milliseconds duration.

The transportation and packaging materials used should ensure that the system components are not exposed to environmental conditions which are more extreme than those specified for storage.



Hardware Configuration and Peripheral Extensions

1.4.3 Conditions for Operation of Units

The system components will operate in environments where the conditions are within the ranges specified in table 1.1. These figures assume that the combined effect of temperature and humidity changes preclude condensation in any part of the unit or on any storage or printing media.

Table 1.1 Conditions for Storage and Operation of Units

temperature range - storage	-40°C to 70°C
- operating	10°C to 35°C
- disks	10°C to 52°C
max temperature change rate	
- storage	5° per minute
	.5° per minute
relative humidity - storage	5% to 95%
- operating	20% to 80%
absolute humidity - storage	less than 35 grms per
	cubic metre
- operating	3 to 20 grms per cubic
. 5	metre
max dew point temperature	28°C
atmospheric pressure	
- storage	45kPa to 110kPa
- operating	
operating	normal max altitude
	2900 metres
non-conductive dust particle	0.5/m 4.10 part/m
size	1/m 4.10 part/m
	5/m 4.10 part/m
gaseous pollution	continuous exposure to sulphur
	dioxide and hydrogen sulphide
	open air concentrations of
	0.1 ppm will not adversly
	affect the operation of
	equipment
sea proximity	the equipment has been
	operated with an air
	concentration of up 2.7/ug of
	salt (NaCl) per cubic metre of
	air

Note: Do not expose the P2000C to strong sunlight.

Hardware Configuration and Peripheral Extensions



SHOCK AND VIBRATION

When operating within a system, the components are able to perform as specified while being subjected to the following shock and vibration limits:

- continuous vibration (i.a.w. IEC 68)
 - 10 through 58 Hz maximum 0.15 mm peak-to-peak
 - 58 through 150 Hz maximum acceleration or deacceleration of $1.96~\text{m/sec}^2$ (0.2g) and $9.81~\text{m/sec}^2$ (1.0g) in 3 axes, 2.0 hr/axis sweep 1 octave/minute
- intermittent shocks
 - up to 9.81 m/sec^2 (lg) and not exceeding 11 milliseconds duration. No shock is to be repeated more than twice per second.

1.4.4 Electromagnetic Constraints

The system components meet the EEC, EFTA and German standards for high frequency appliances.

Tested against Funk-Störvorschrift ÖVE F62, Klasse B.)

1.4.5 Electrostatic Constraints

The system components and total system have been designed in such a way as not to be harmed by static discharge during normal operation, although users should ensure that they do not have a static charge before touching PCB's.

1.4.6 Positioning of P2000C

The P2000C is designed to operate correctly on a table-top, with the tilt-bar extended to improve the viewing angle. If the equipment is used with the tilt-bar folded, adequate space should be allowed for air convection. Under no circumstances should it be operated in any other position, which could interfere with the operation of the disk drives.





Detailed Description and Servicing Introduction

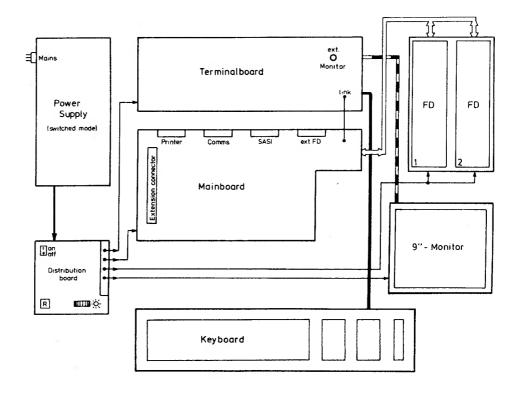
1 GENERAL

The P2000C consists of the following main units:

- Power Supply Unit and Distribution Board
- Mainboard
- Terminalboard
- 9" Monitor
- Two 5%" Flexible Disk Drives (160 Kbytes or 640 KBytes)
- Keyboard

With the exception of the Keyboard, all the units are contained within the main casing.

The integration of the various units is shown in the following block diagram:



Detailed Description and Servicing Introduction



2 P2000C 12NC NUMBERS

To clarify the significance of the numbers that you will find on PCB'S inside the unit, an example is shown below.

2.1 Example

The component side of the Mainboard, shown on the following page, has the numbers:

- a) 5103 103 3114.1
- b) 8203 235 0591.1
- c) 8203 235 0594.1
- d) 8203 235 0593.1
- e) 0271.1

These numbers should be interpreted in the following way:

- a) Read as 5103 103 3114 'point' 1 (medium significance)
 This is the number of the printed board, the 1 following the
 point representing the status of the printed board.
- b) Read as 8203 235 0591 'point' 1 (low significance)
 This is the number of the component side layout, once again
 the digit following the point representing the status of the
 layout.

Both of the above numbers are etched onto the board in the same way as the printed track.

- c) Read as 8203 235 0594 'point' 1 (low significance)
 This is the number, including status (point number), of the
 Service Printout. It is printed in white on the board.
- d) Read as 8203 235 0593 'point' 1 (low significance)
 This is the number, including status (point number), of the solder resist varnish layout. This number is stamped into the varnish.
- e) Read as (5103 108) 0271 'point' 1 (high significance)
 This number, the ASSY NUMBER, with the implied 5103 108,
 represents the 12 NC number of the complete assembly. The
 point number gives the status of the assembly. This number
 is printed on a white 'stick-on' label.
 The 'point number' of each main assembly is repeated on the
 Service Sticker on the outside of the P2000C.

The numbers described at b) and d) above are also found on the solder side of the PCB.





Detailed Description and Servicing Introduction

Service Sticker 2.2

The Service Sticker, shown below, is attached to the underside of the P2000C. It is used to indicate the modification status of all the main assemblies incorporated in the machine. The modification status should be taken as the highest number 'blocked-out'. This number corresponds to the 'point-number' in the ASSY number (see 2.1, e).

P2000C PORTABLE COMPUTER									PHILIPS
UNIT	MODIFICATION S	ERVICE							SERVICE
MONITOR	23456789		TERMPCB					89	
POWER SUPPLY	23456789		KEYBOARD-PCB	1	3	4 5	67	89	
DISTRIBUTPCB	23456789		EXTENSPCB					89	
MAIN-PCB	12456789			1 2	23	<u>4 5</u>	_	89	
170 (0.7.1.)								5103	3 106 0707.3

The above example would represent a P2000C containing:

- Monitor	Status 1	- release status
- Power Supply	Status 1	- release status
- Distribution PCB	Status 1	- release status
- Mainboard PCB	Status 3	- two modifications incorporated
	Status 2	- one modification incorporated

one modification incorporated - Terminalboard PCB Status 2 - Keyboard PCB Status 2 - one modification incorporated
- Extension PCB Not fitted

Detailed Description and Servicing Introduction



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Detailed Description and Servicing Power Supply

1 GENERAL

The P2000C Power Supply Unit has been designed to be serviced by replacement at first line, with factory repair facilities. For this reason this chapter will only outline the basic specification of the unit to give information for testing, on a GO/NO GO basis.

2 SPECIFICATION

Nominal output power:
AC input voltage
(selectable by jumper):
DC output voltages:

Max power on all DC outputs

82 W 90 - 140V 47-66 Hz 180 - 264V 47-66 Hz

REF	VOLTAGE	ON PINS	GND PINS	Remarks
V1	+5	11,12,13	8,9,10	TTL supply voltage
				2 - 6A, $+/- 3%$
V2	+12	6,7	4,5	0.1 - 2.8A, +/- 5% maximum
				3.8A for less than 40 ms,
				+/-10%
V3	+12	3	4,5	Monitor supply voltage
				0 - 1.2A, +/- 1% (series
				regulated) ripple
				synchronous to mains
				frequency must be less than
/	1.0	•	,	30mV peak to peak.
V 4	-12	2	4,5	RS 232 supply voltage
				0 - 0.3A, +/- 5%
Rin	ple and n	nise		2% max (except V3)
_	iciency	0100		75% min
	•	protection	on V1	For voltages greater than
OVE	Ivortage	protection	OH VI	6.2V +/- 0.4V
Sho	rt circui	t protecti	on	Maximum short circuit
on .	all DC ou	tputs.		currents
				(V1) 6A
				(V2) 3A
				(V3) 3A
				(V4) 2A
0ve	rcurrent	protection	•	
		11		0 =

95W

Detailed Description and Servicing Power Supply



3 SAFETY PRECAUTIONS

3.1 Mains Input Plug

Mains input filters are included in the primary circuit of the power supply unit to reduce, for example, the chances of mains spikes being fed into the P2000C and producing unwanted results. Due to these filters, the removal of the mains plug while the machine is still switched on results in a high voltage being across the pins of the input plug for some time.

WARNING

ALWAYS SWITCH OFF BEFORE REMOVING THE MAINS PLUG

3.2 High Voltage Warning

HIGH VOLTAGE WARNING

VOLTAGES OF UP TO 800V ARE PRESENT IN THIS UNIT

The P2000C must not be operated with the cover removed.

Dangerous voltages of up to 800 VOLTS are present in the vicinity of the power transistor, including THE POWER TRANSISTOR HEAT SINK.

Dangerous voltages in excess of 42V are present at various points of the power supply unit.





4

Detailed Description and Servicing Power Supply

INPUT VOLTAGE SELECTION

WARNING

No attempt must be made to carry out this procedure with power applied to the equipment. Remove the power cable first.

The power supply unit is designed to operate at either:

- 90V - 140V 47 - 66Hz (nominal 115V) - 180V - 264V 47 - 66Hz (nominal 230V)

The unit will be set to the correct input for local conditions but should it be necessary to change the input voltage the following procedure should be carried out:

- Remove the power supply unit as described in Part 4.
- Identify the flying lead that will be connected to one of the two input pins marked:

115V or 230V

11 o

- Ensure that the flying lead is connected to the input pin appropriate to local conditions
- Refit the power supply unit as described in Part 4

Detailed Description and Servicing Power Supply



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Detailed Description and Servicing Mainboard - Introduction

1 GENERAL

The P2000C Mainboard contains the following main functional blocks:

- 4 MHz Z80-A CPU
- Direct Memory Access
- DATA and ADDRESS Buffers
- Clock Generator
- I/O Decoder
- Memory Manager
- 64 Kb Dynamic RAM's
- Initial Program Load (IPL) ROM
- Shugart Associates Standard Interface (SASI)
- FD-Controller for 5" flexible disks
- CTC Baudrate Generator
- 3 Full Duplex Serial Channels (synchronous or asynchronous)
- Bus connector for a possible system extension

Detailed Description and Servicing Mainboard - Introduction



2 SIGNALS

2.1 External Signals

Pin designation of the main bus (connector PB) is shown in table 2.17 (Bus Extension). Other external connections to the Mainboard are shown in the following tables (2.1 to 2.9).

Table 2.1 SASI Connections (PSA)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
02	D00	14	D06	42	MSG-N
04	DO1	16	D07	44	SEL-N
06	D02	36	BSY-N	46	C-N/D
08	D03	38	ACK-N	48	REQ-N
10	D04	40	RES-N	50	1/0
12	D05				·

PINS 1, 3, 5...49, 18, 20, 22...34 - GND

Table 2.2 54" FDC Connections (PFD)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
02	SPARE	14	DS3	26	TRKO
04	HEAD LOAD/IN US	SE 16	MOTON	28	WRT.PR.
06	DS4	18	DIRECTION	30	RDD
80	INDEX	20	STEP	32	SIDE SELECT
10	DS1	22	WRITE DATA	34	READY
12	DS2	24	WRT.GT.		

PINS 1, 3, 5...33, - GND

Table 2.3 External Terminal Connections (PSE 1)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
02 03	TxD RxD	05 06	CTS DSR	15 20	ASYN O
04	RTS	06	GND	20	DIK

Other pins - Not Connected



Detailed Description and Servicing Mainboard - Introduction

Table 2.4 Communications Connections (PSE 2)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
02	TxD	06	DSR	17	ECLK 2
03	RxD	07	GND	20	DTR
04	RTS	08	DCD	24	ECLK 0
05	CTS	15	ECLK 1	25	ECLK 3

Other pins - Not Connected

Table 2.5 Printer Connections (PSE 3)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
02 03 04	TxD RxD RTS	05 06	CTS DSR	07 20	GND DTR

Other pins - Not Connected

Table 2.6 Internal Serial Interface Connections (PSE 0)

PIN	SIGNAL	PI	N SIGNAI	PIN	SIGNAL
01 02	TxD-N RxD-N	0	·	05 06	ASYN O GND

Table 2.7 RESET Connections (PR)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
01 02	SRES-N SRES-N	03	GND	04	NMI-N

Table 2.8 Power Supply Connections (P1)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
	GND GND		+5 V +5 V		+12 V +12 V	•	-12 V -12 V

Table 2.9 Optional Sound Source Connection (PC)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
01	+ 5V	02	GND	03	CTC 2 TCO O/P

Detailed Description and Servicing Mainboard - Introduction



2.2 Mainboard Bus Signals

Signals are carried on a series of busses between different elements of the Mainboard, the Terminalboard, and the Extension connector. The busses to be found on the Mainboard are as follows:

BUS NAME	SIGNALS
IO D-BUS	IODO - IOD7
DATA BUS	IDO - ID17
ASYN BUS	ASYNO - ASYN3
AD BUS	ABO - AB15
MEM AD BUS	MAO - MA7
CS BUS	Chip Select Signals
CNTR BUS	Control Signals

The Chip Select signals are detailed in table 2.10. The Control signals are detailed in table 2.11.

Table 2.10 P2000C Mainboard - Chip Select Signals

SIGNAL	SELECTS
CSO-N	DRQ1
CS2-N	USART
CS3-N	SASI
CS4-N	SASI
CS5-N	FD Controller
CS8-N	CTC1
CS9-N	CTC2
CSA-N	SIO
CSMM-N	Memory Manager
CSFD-N	Output Port
CSDMA-N	Direct Memory Access





Detailed Description and Servicing Mainboard - Introduction

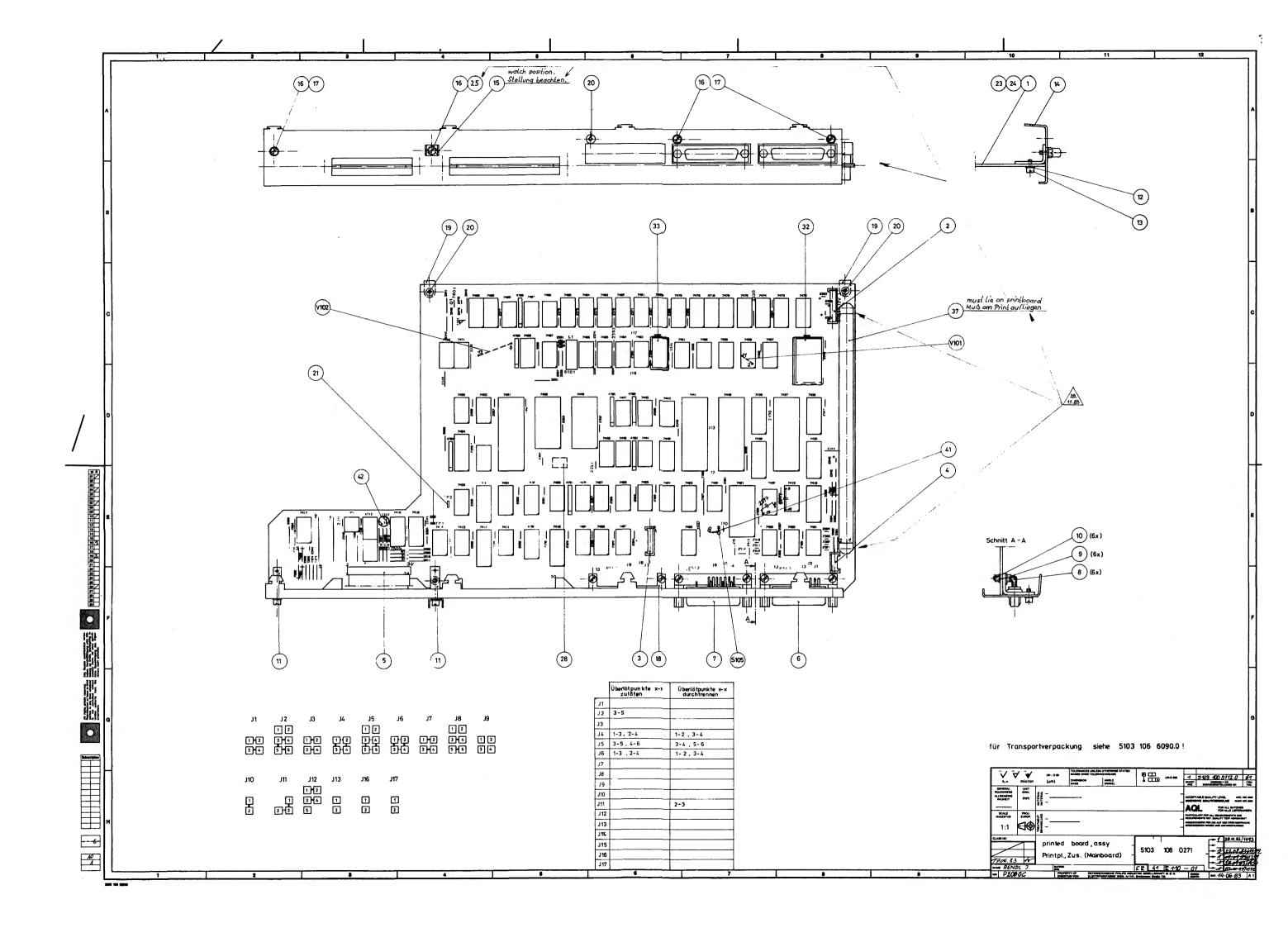
Table 2.11 P2000C Mainboard - Control Bus Signals

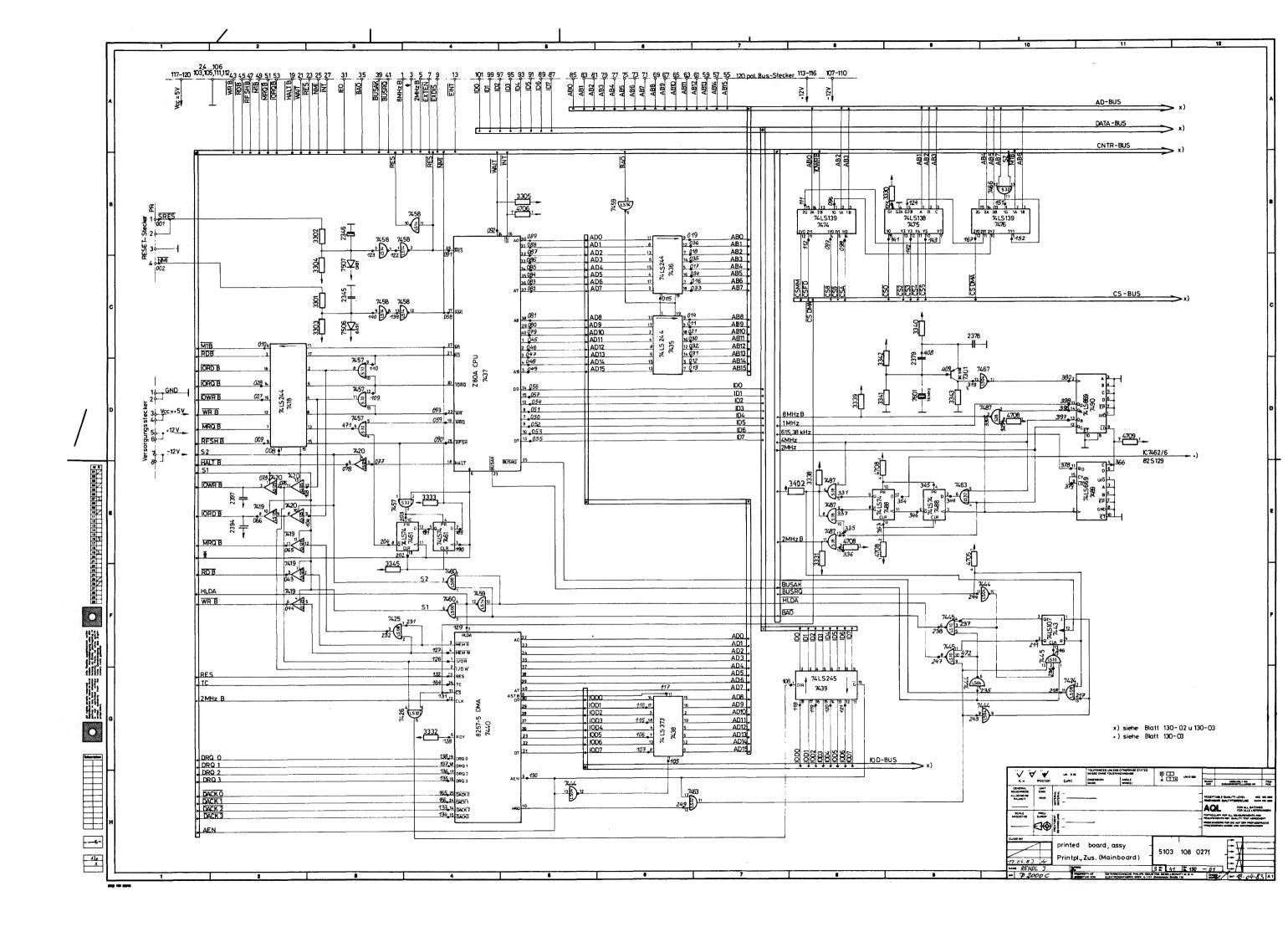
SIGNAL	DESCRIPTION
M1 B-N	Machine Cycle 1-Buffered (inverted)
S1	DMA/CPU
S2	DMA/CPU - Slave/Master
▼ (Clock)	System Clock
615.38 KHz	Timing Signal
1 MHz	Timing Signal
2 MHz	Timing Signal
2 MHz B	Timing Signal
4 MHz	Timing Signal
8 MHz B	Timing Signal
BUSAK-N	Bus Acknowledge (inverted)
BUSRQ-N	Bus Request (inverted)
BAO-N	Bus Acknowledge Out (inverted)
INT-N	Interrupt (inverted)
WAIT-N	Wait (inverted)
NMI-N	Non Maskable Interrupt (inverted)
RES	Reset
RES-N	Reset (inverted)
IORQB-N	I/O Request (inverted)
IORDB-N	I/O Read (inverted)
IOWRB-N	I/O Write (inverted)
RDB-N	Read (inverted)
WRB-N	Write (inverted)
MRQB-N	Memory Request (inverted)
RFSHB-N	Refresh (inverted)
HALTB-N	Halt (inverted)
HLDA	Hold Acknowledge
TC	Terminal Count
DRQO	Data Request 0
DRQ1	Data Request 1
DRQ2	Data Request 2
DRQ3	Data Request 3
DACKO-N	Data Acknowledge 0 (inverted)
DACK1-N	Data Acknowledge 1 (inverted)
DACK2-N	Data Acknowledge 2 (inverted)
DACK3-N	Data Acknowledge 3 (inverted)
IEIS	Interrupt Enable CTC 1 Address Enable
AEN	
IEO	Interrupt Enable Out
EXTEN-N	Extension (Memory) (inverted) Disable Internal ROM (inverted)
EXDIS-N	External Interrupt
EINT	External Interrupt External Interrupt (inverted)
EINT-N	evectuar interrubt (Inverted)

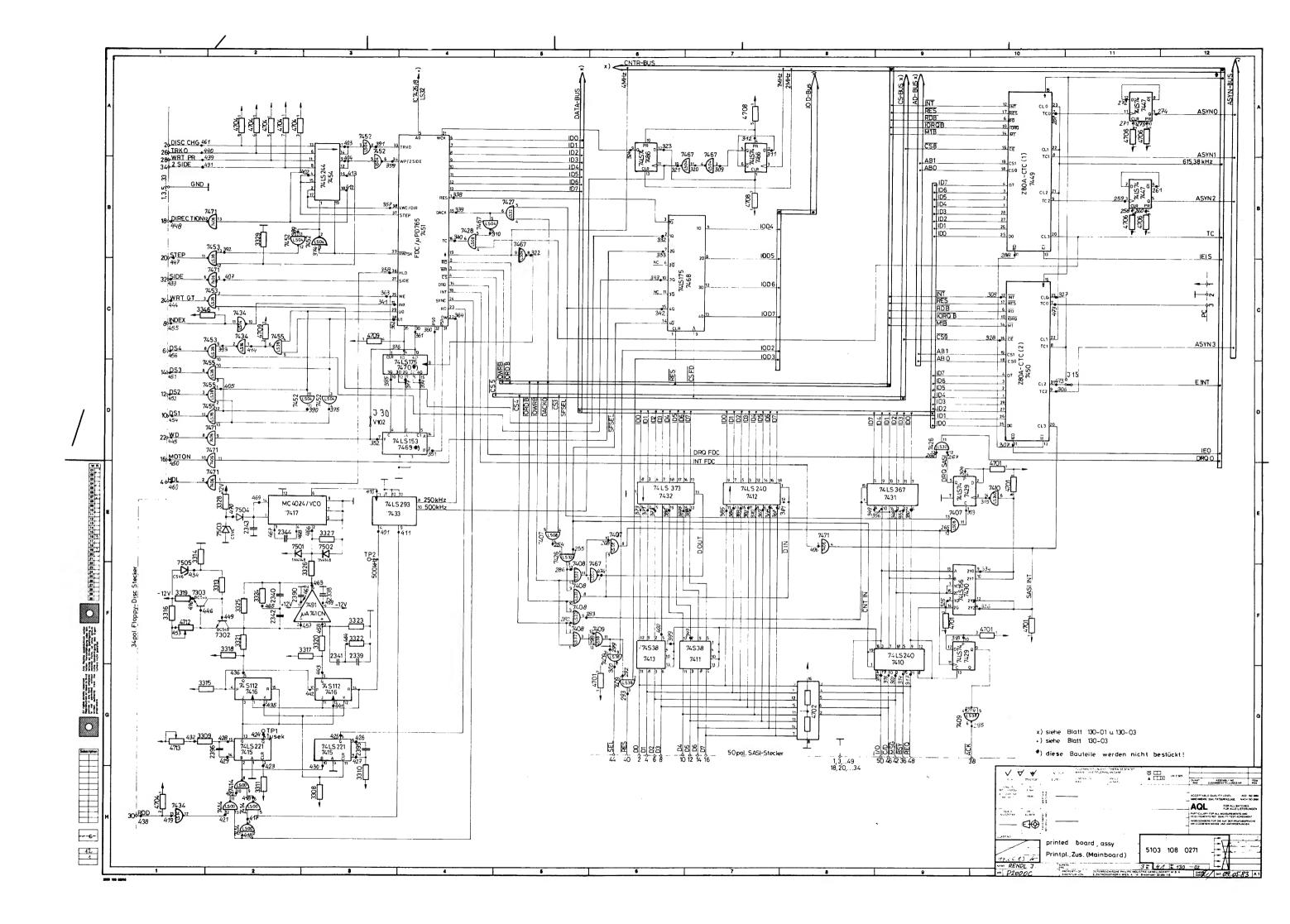
Detailed Description and Servicing Mainboard - Introduction

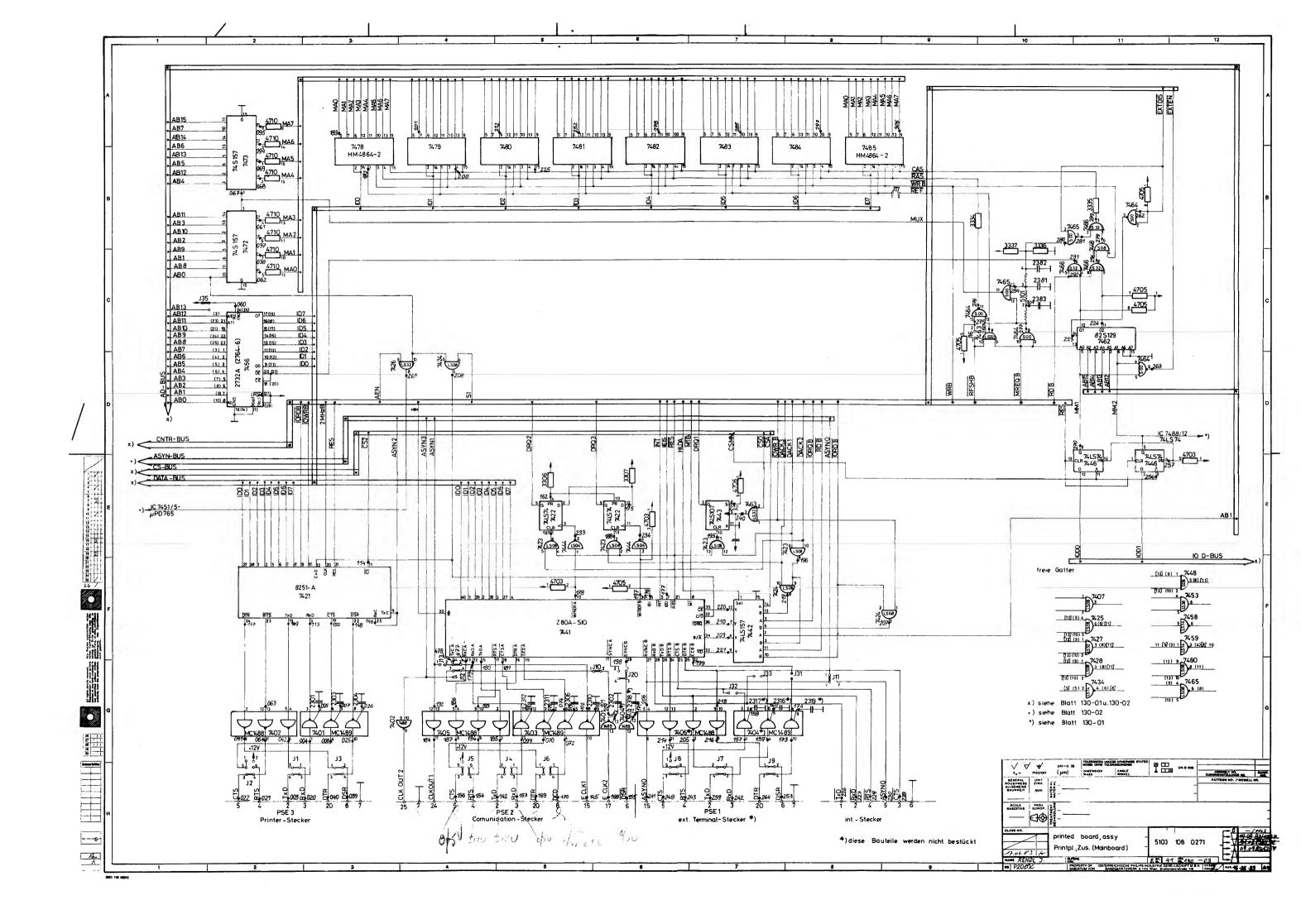


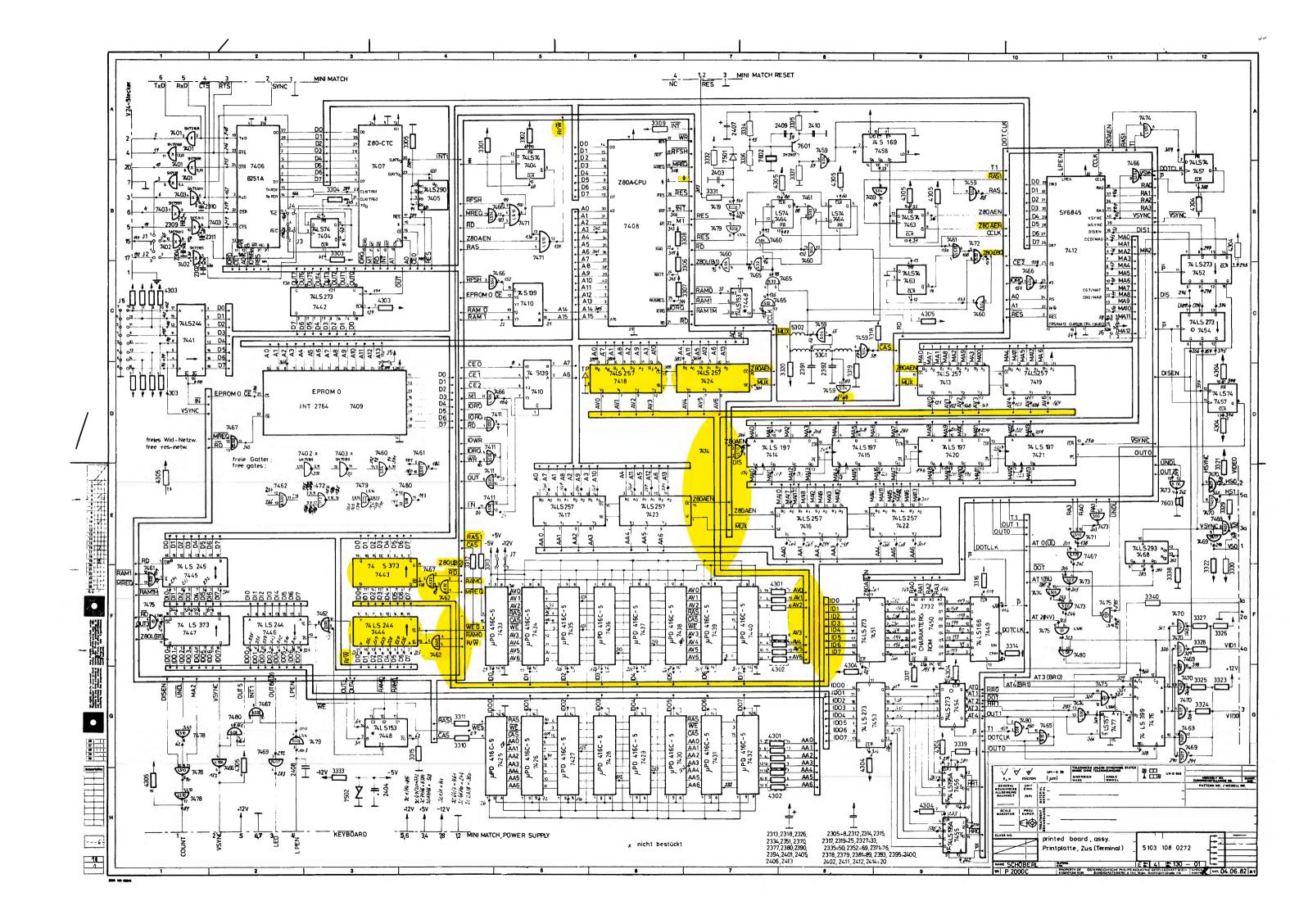
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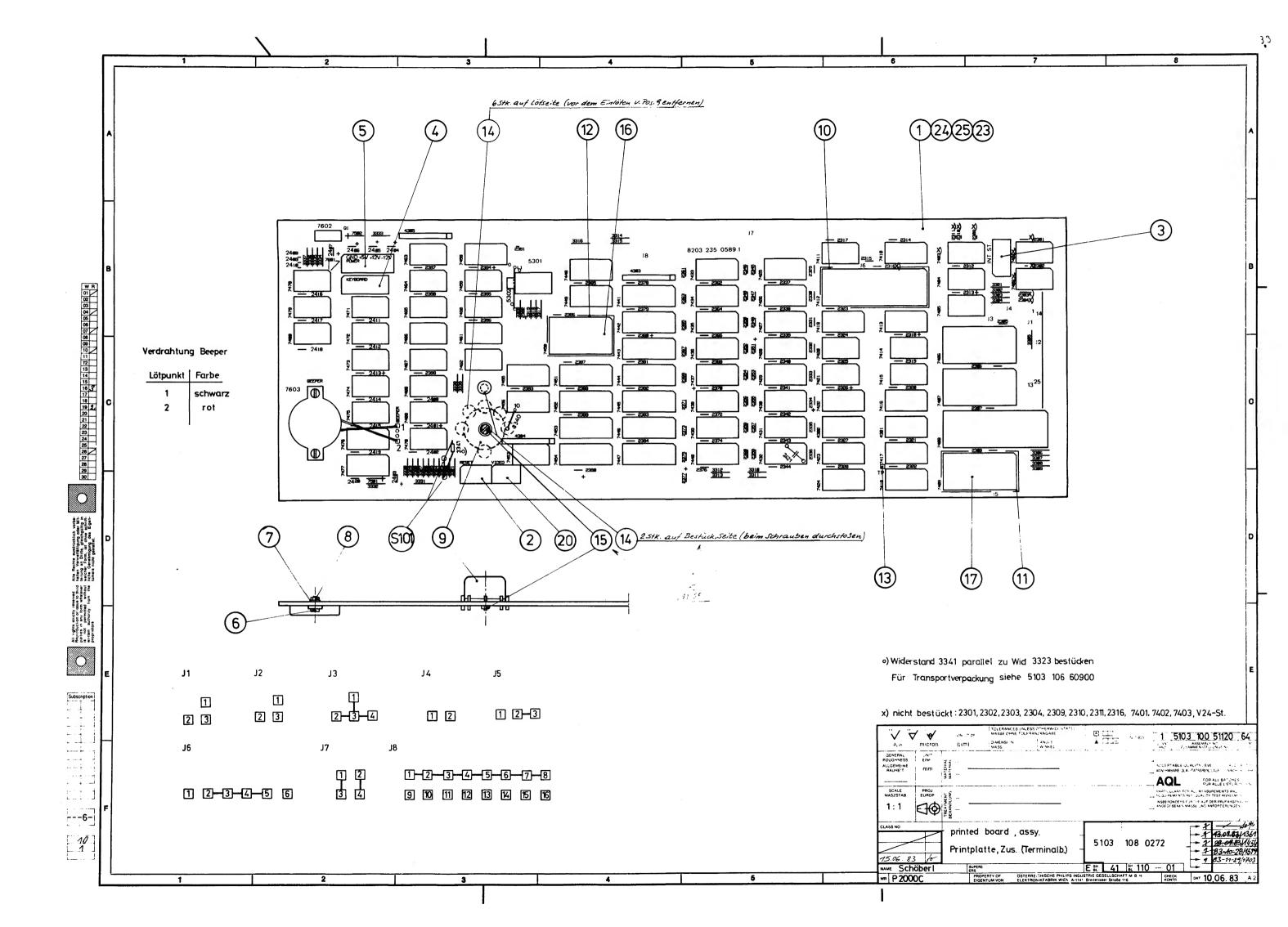














1

Detailed Description and Servicing Mainboard - CPU

GENERAL

The Z80A CPU, a third generation single-chip microprocessor with exceptional computational power, offers higher system throughput and more efficient memory utilization than comparable second and third generation microprocessors. The internal registers contain 208 bits of read/write memory accessible to the programmer, including 2 sets of 6 general purpose registers which may be used individually as 8 bit registers or as 16 bit register pairs, and 2 sets of accumulator and flag registers. An 'exchange' instruction set makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or may be reserved for very fast interrupt response. The Z80A contains Stack Pointer, Program Counter, 2 Index Registers, a Refresh Register (counter), and an Interrupt Register. Output signals are fully decoded and timed to control standard memory or peripheral circuits. The Z80A is supported by an extensive family of peripheral controllers. Figure 2.1 shows the main functions. Full details of the Z80A CPU can be found in the Z80A Mostek 1979 Microcomputer Components Data Sheets

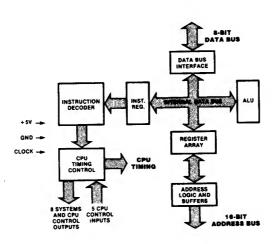


Figure 2.1 Z80A CPU - Block Diagram

In the P2000C, the Z80A CPU operates at a frequency of 4 MHz when working with RAM, and is switched to 2 MHz when working with additional ROM. (See also Chapter 2.4 - Clock Generator).

Detailed Description and Servicing Mainboard - CPU



2 BLOCK DIAGRAM

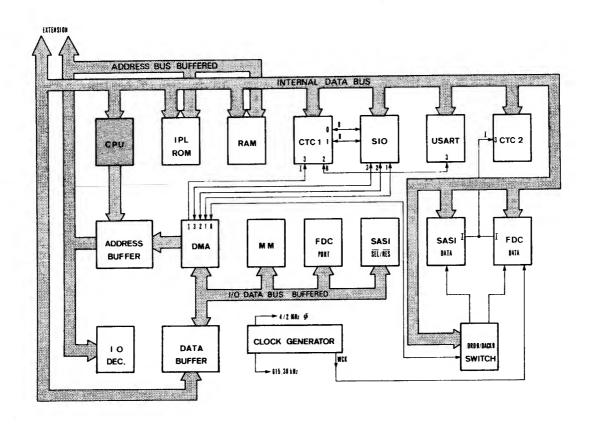


Figure 2.2 P2000C - CPU Block Diagram



Detailed Description and Servicing Mainboard - CPU

3 CIRCUIT DESCRIPTIONS

3.1 Data Bus and Address Bus

As shown in figure 2.2, the system data bus is partly buffered. Although the CPU (item 7437) is able to drive four LS TTL loads, this buffering ensures that a maximum of three loads are on the data bus at any time. The Address bus is fully buffered. The CPU address bus and the DMA address lines are simultaneously buffered by the same two I.C. drivers 74 LS 244 (items 7435/7436).

3.2 Control Bus

Two components on the Mainboard (DMA and USART) require special compound signals, which are produced by items 7457, 7419 and 7420 as follows:

IORD-N signal formed from the RD-N & IORQ-N signals. IOWR-N signal formed from the WR-N & IORQ-N signals.

In order to prevent any possibility of timing problems between a RAM access and a Refresh, the MREQ-N signal is "precharged" using a circuit consisting of two D-FF's (Item 7461).

RAS Precharge Time - worst case = 60 ns.

Precharge logic timing is shown with the DMA/CPU Timing Diagram on page 3.2 3-6.

Note: This circuit only functions during an Opcode fetch (activated by M1-N). Correct function is only guaranteed if no wait states are used. In memory write or read and I/O cycles, this circuit remains idle.

The Control Bus signals are fully buffered.

For situation of CPU in relation to other Mainboard circuits, please refer to the full circuit diagrams.

Detailed Description and Servicing Mainboard - CPU



3.3 Additional Signals

The signals RES-N and NMI-N can be activated by external debounced switches. Only the RESET switch is implemented. At each power-up the RES-N signal is automatically activated. The signal NMI-N is also activated during the power up phase but is of shorter duration (due to the use of a smaller CR time constant) than the RESET and does not affect the CPU operation.

The DMA is programmed by, and works under the control of, the CPU. A handshake routine, in the form of a simple data exchange, is used to allocate use of the data bus to the DMA as required and to ensure that only one device attempts to use the bus at any time. BUSAK-N controls the tristate outputs of the Bus buffer, offering a high impedance to the bus. BUSAK-N and BUSRQ-N work with the 8257 DMA. Both of these signals are available on the Bus plug.

The priority logic ensures that internal DMA (bus request HRQ) has priority over additional, external DMA on the bus extension (bus request BRE), in the event of contention. However, once either internal or external DMA has initiated a transfer, no interruption is allowed.

The Z80A can be used in three interrupt modes - 0, 1 and 2. The P2000C uses Interrupt mode 2, which is supported by two CTCs (used as Interrupt controllers) and the SIO. If the basic unit is extended, via the 120 way Bus plug, only one additional Z80 Interrupt device is allowed. This is because a maximum of four devices are allowed with the 4 MHz configuration due to delay times in the interrupt daisy chain. Further details of the Z80A Interrupt Modes are given in the CPU Data Sheet.

The Wait line is not used on the Mainboard, and must not be used on the optional extension board in combination with an Opcode fetch cycle. It can be used on the extension board to slow down I/O transfers when working with slower devices.



1

Detailed Description and Servicing Mainboard - DMA

GENERAL

The Intel 8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus is accomplished via the CPUs hold function. The 8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the CPU that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The 8257 greatly simplifies the transfer of data at high speed between peripherals and memories.

Full details of the Intel 8257 DMA can be found in the Intel Component Data Catalogue 1981.

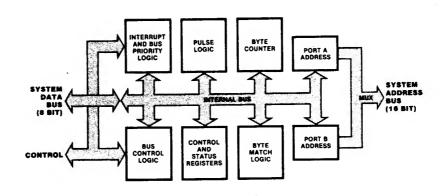


Figure 2.3 8257 DMA - Block Diagram

2

Detailed Description and Servicing Mainboard - DMA



In the P2000C, the 8257 DMA Controller operates at a frequency of 2 MHz. It controls transfers from Memory to I/O and I/O to Memory in four channels (0 to 3).

The DMA operates in either Master or Slave mode. In the Slave mode the CPU has full control of the Address, Data and Control bus, and prepares the DMA for later transfers of data. Once control has been handed to the DMA, switching it to Master mode, it controls the transfer of data directly between the I/O device and memory by the use of DACK-N signals.

BLOCK DIAGRAM

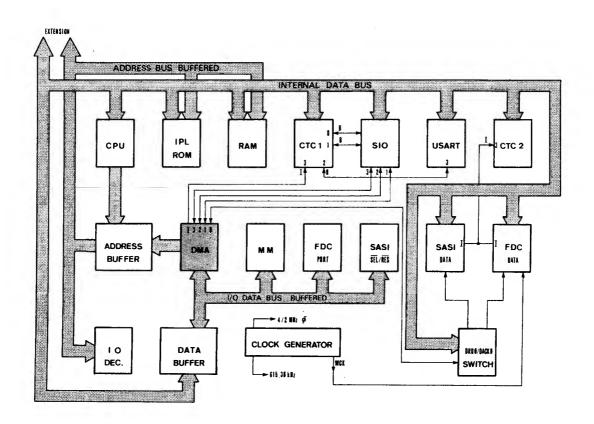


Figure 2.4 P2000C - DMA Block Diagram



Detailed Description and Servicing Mainboard - DMA

3 CIRCUIT DESCRIPTIONS

3.1 Data Transfer

The DMA Controller (item 7440) only generates the addresses and control signals required to transfer the data between memory and the I/O. No intermediate storage is involved and the data is not routed through the controller. For this reason the DMA Chip can operate on the I/O Data bus while the addressed I/O devices are operating on the internal Data bus.

Each channel has a DRQ input from the I/O Device and a DACK-N output to the I/O Device. Channel O has the highest priority when the Rotating Priority Mode bit is not set to zero.

Channel O has two possible uses. Selection can be made, via the output board 1FH bit 7 (FDC Port), between:

Note: The selection has to be defined by software, to ensure that only the correct unit can demand a DMA Cycle, and the FDC <u>must</u> be reset before the SASI is selected.

Table 2.12 - Distribution of the DMA Channels

CHANNEL	DESTINATION	PURPOSE
0	FDC or SASI	Data Transfer
1	SIO Channel A	Communication
2	SIO Channel A	Communication
3	SIO Channel B	Terminal

The control signals of the DMA-Controller are buffered. The circuitry ensures that these buffers are correctly controlled to avoid bus conflict. This is achieved with the Priority Logic circuit which produces the HLDA-N and BAO-N from the HRQ, AEN, BUSACK-N, BUSRQ-N and system clock signals (items 7443, 7444, 7445, 7424 and 7463).

DMA address lines and the CPU address bus are simultaneously buffered by the same two I.C. drivers 74 LS 244 (items 7435/6).

Detailed Description and Servicing Mainboard - DMA



3.2 Multiplexed Address/Data Bus

The address strobe is used to store the addresses in the transparent D-latch 74 LS 373 (item 7438), where the higher addresses are formed.

3.3 Software Considerations

The DMA always works in the Single Byte Mode. This ensures that the RAM's will be refreshed correctly. When the FDC DMA Channel is active, timing problems may be caused by using the Rotating Priority Mode.

The SIO has only one ready signal for each channel which can be used as DRQ signal for the DMA. To make it possible to drive the communications interface via DMA in both directions (receiver and transmitter), an artificial DRQ signal must be generated for one direction. This is achieved in the following way:

- The DMA chip must first be programmed (slave mode). If a data transfer has to be carried out, the SIO triggers an interrupt. Only one Out-command to address 10H or 11H is necessary (in the Interrupt Service Routine) to start the data transfer. The SIO programming defines whether this procedure is to be used for transmitting or receiving data. This is much faster than the complete treatment with software.

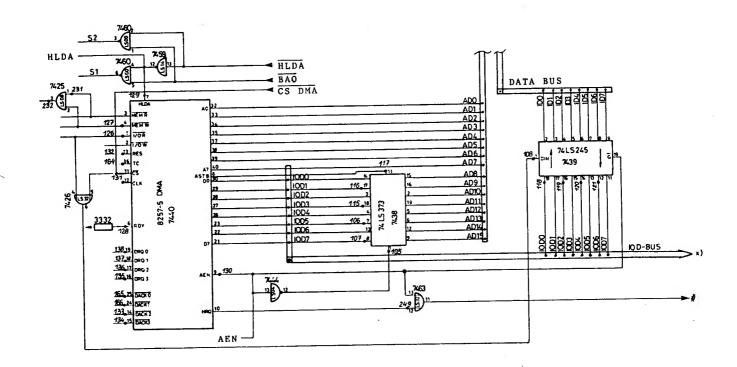
If transmission and reception are at different baud rates, it is advisable that the faster process should use the W/RDY pin on the SIO to start the DMA transfer. This will minimise the effect of using the above process. (See Note below).

At the terminal interface you can also select, by Software, whether the Receiver or the Transmitter shall be processed by DMA.

Note: Even if transmission and reception are at the same baud rate, the programmer should decide which direction is more time critical.



Detailed Description and Servicing Mainboard - DMA



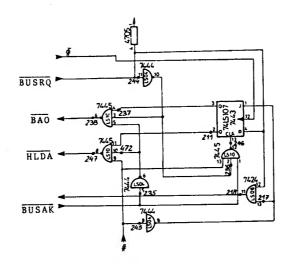
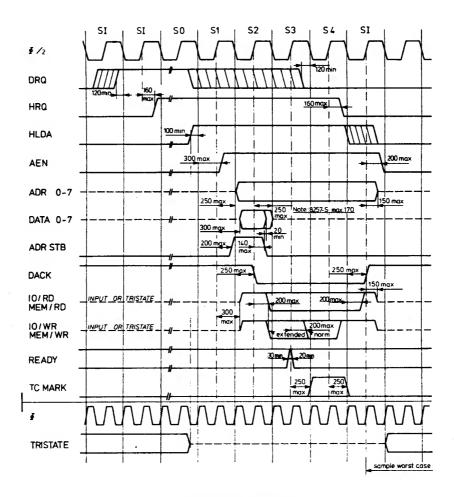


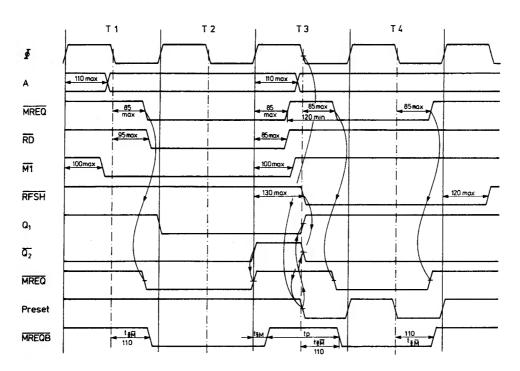
Figure 2.5 Circuit Diagram - DMA

Detailed Description and Servicing Mainboard - DMA





DMA/CPU Timing



Memory Request Precharge Logic Timing



Detailed Description and Servicing Mainboard - DATA/ADDRESS Buffers

1 GENERAL

The system data bus is partly buffered, and is capable of handling a maximum of 3 TTL LS loads. The component used for this function is a bi-directional selectable latch/buffer. The address bus is fully buffered. The CPU address bus and the DMA address lines are simultaneously buffered.

2 BLOCK DIAGRAM

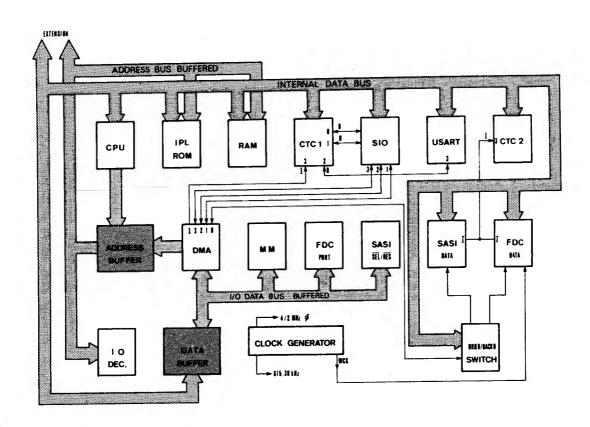


Figure 2.6 P2000C - DATA/ADDRESS Buffers Block Diagram

Detailed Description and Servicing Mainboard - DATA/ADDRESS Buffers



3 CIRCUIT DESCRIPTION

The bi-directional latch 74 LS 245 (item 7439) is controlled by a signal which is derived, via an OR-gate (item 7426), from the DMA signals CS-N or I/OR-N. The two 74 LS 244 (items 7435/7436) are used as address bus buffers.

3.1 Internal Data Bus - Loading

The following tables show the maximum resistive and capacitive loadings for the internal data bus:

RESISTIVE LOADING

	IDO	ID1	ID2	ID3	ID4	ID5	ID6	ID7
Bus buffer	+	+	+	+	+	+	+	+
SASI data out	+	+	+	+	+	+	+	+
Optional exten	+	+	+	+	+	+	+	+
Maximum 3 LS TTL	loads							

CAPACITIVE LOADING

	60pF
	12pF
	7pF
	40pF
(1)	5pF
(2)	10pF
(1)	5pF
(1)	5pF
ve load	144pF
	(2) (1) (1)





Detailed Description and Servicing Mainboard - DATA Buffers

3.2 I/O Data Bus - Loading

The following tables show the maximum resistive and capacitive loadings for the I/O data bus:

RESISTIVE LOADING

	IDO	ID1	ID2	ID3	ID4	ID5	ID6	ID7
DMA latch	+	+	+	+	+	+	+	+
Memory manager	+	+	+	+				
FDC Out Port					+	+	+	+
SASI SEL, RES			+	+				
Maximum 3 LS T7	TL load	ls						

CAPACITIVE LOADING

DMA chip		20pF
TTL at 5pF		
DMA latch	(1)	5pF
Memory manager	r &	
FDC Port	(1)	5pF
Buffer	(1)	5pF
SASI SEL, RES	(1)	5pF
Total capacitive		40pF

Detailed Description and Servicing Mainboard - DATA Buffers



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1

Detailed Description and Servicing Mainboard - Clock Generator

GENERAL

All frequencies which are needed on the Mainboard are produced by the Clock Generator, including some special signals:

16 MHz
8 MHz
4 MHz
2 MHz
1 MHz
615,38 kHz
Write clock for the FDC (WCK)

2 BLOCK DIAGRAM

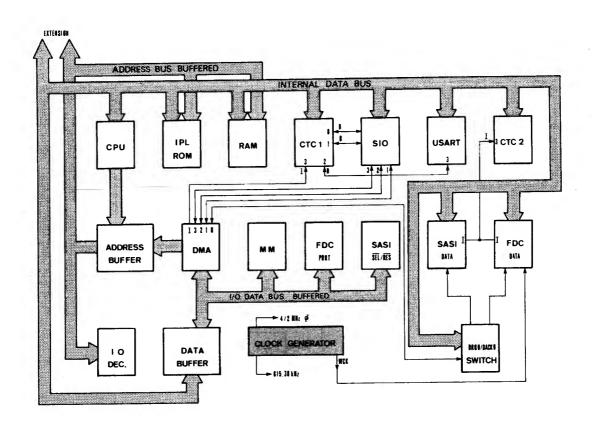


Figure 2.7 P2000C - Clock Generator Block Diagram

3

Detailed Description and Servicing Mainboard - Clock Generator



CIRCUIT DESCRIPTION

A quartz stabilised Colpits-Oscillator generates a frequency of 16 MHz. It is followed by a TTL-buffer (item 7467) with a Schmitt-trigger input. The outputs are obtained, by division, from a 4 bit binary counter (items 7489/7490). See figure 2.10.

The 4 MHz signal is used as the system clock. Due to the use of slower ROMs, the system clock is switched over to 2 MHz when the Memory Manager accesses ROM. (MM2 = 0). The circuit with two flip-flops (item 7488) ensures that no spikes can be produced in the clock during switch over. (Both input clocks are "0" during the switch-over, making the following Open Collector Drivers (item 7487) inactive.) (See Timing Diagram - A)

The 8 MHz signal is used to clock a second 4 bit counter. It is wired to count down from 12 to 0 in order to create the input frequency of 615.38 kHz used for the Baud Rate Generators. (Note: 19 200 x 32 = 614.4 kHz, a deviation of 0.16%). (See Timing Diagram - B)

The 1 MHz signal is used to generate an asynchronous 500 kHz signal (2us cycle-time). This signal is combined with the 2 MHz signal (250 ns one half-cycle) to produce the timing for the Floppy Disk Write Clock WCK (using item 7486). The two inverters (item 7467) are used to delay the 500 KHz signal to avoid spikes in the WCK signal. (See Timing Diagram - C)

Timing diagrams for the Mainboard Clock Generator are shown in figure 2.9.

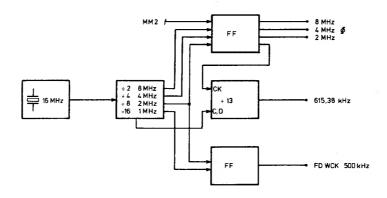
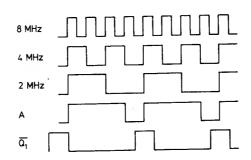


Figure 2.8 Clock Generator - Detailed Block Diagram

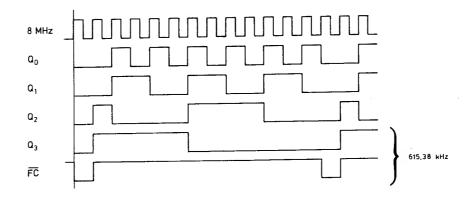


Detailed Description and Servicing Mainboard - Clock Generator

A - System Clock



B - Baudrate Generation



C - FDC WCK Generation

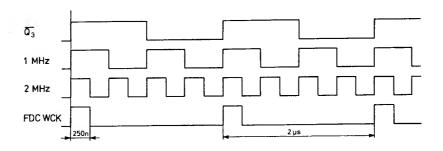


Figure 2.9 P2000C Clock Generator - Timing Diagrams

Detailed Description and Servicing Mainboard - Clock Generator



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Detailed Description and Servicing Mainboard - Clock Generator

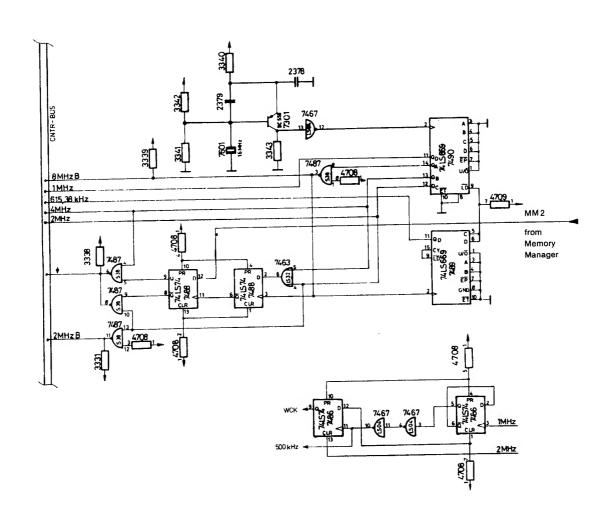


Figure 2.10 Circuit Diagram - Clock Generator

Detailed Description and Servicing Mainboard - Clock Generator



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Detailed Description and Servicing Mainboard - I/O Decoder

1 GENERAL

The I/O addresses are hard wired on the Mainboard. They are fully decoded, thus eliminating bus problems if the I/O is extended.

The I/O decoder handles the lower addresses (ABO to AB7) and the bus control signals, in connection with DMA activities. The IORQB-N signal must be gated separately on each I/O component.

The decoder output signals are used as the chip select signals for the I/O devices.

BLOCK DIAGRAM

2

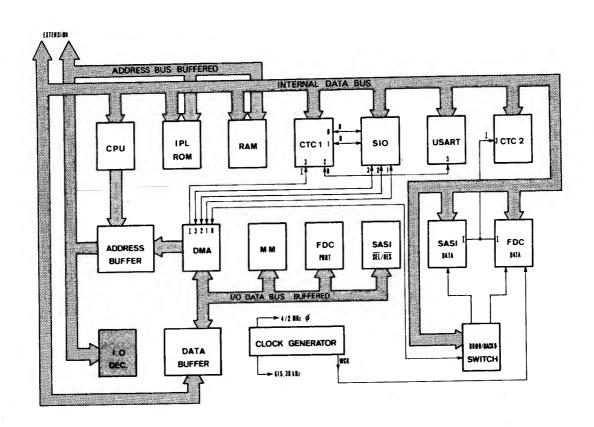


Figure 2.11 P2000C - I/O Decoder Block Diagram

Detailed Description and Servicing Mainboard - I/O Decoder



3 CIRCUIT DESCRIPTION

Item 7476 is a dual 1 of 4 decoder. Providing that no DMA device is active and that there is no Interrupt Acknowledge Cycle in progress, active low states on AB6 and AB7 cause the 1Y1 output of item 7476 to be active low. This output enables the second half of item 7476 to decode AB4 and AB5, driving one of the three outputs 2Y0 to 2Y2 to active low. See figure 2.12

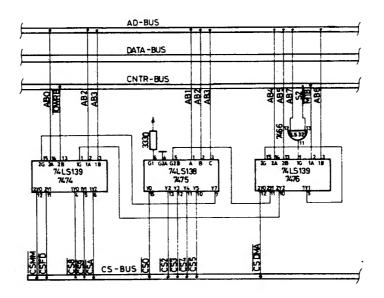


Figure 2.12 Circuit Diagram - I/O Decoder

If 2YO is active, then the DMA chip select — CSDMA-N — is active.

If 2Y1 is active (AB4=1, AB5=0, 1Y1=0), the signal is used to enable item 7475, a 1 of 8 decoder.

If 2Y2 is active (AB4=0, AB5=1, 1Y1=0), the signal is used to enable item 7474, the first part of a dual 1 of 4 decoder.

With 2Y1 active, item 7475 decodes AB1 to AB3. In this case, AB1 to AB3 (with address line AB0 wired to the devices) give the majority of the I/O addresses in the range 10H to 1FH. The exceptions are the I/O addresses 1EH and 1FH. In these cases, high states on all three inputs make the output Y7 active, which in turn activates the second part of item 7474. In this case, ABO and IOWRB-N are decoded to produce chip select signals for either Memory Manager (CSMM-N) or Flexible Disk Port (CSFD-N).

With 2Y2 active, the first part of item 7474 decodes AB2 and AB3. With ABO and AB1 wired to the devices, this gives all addresses in the range 20H to 2FH.





Detailed Description and Servicing Mainboard - I/O Decoder

The decoding is shown table 2.13:

Table 2.13 - I/O Decoding

IF ABO-AB7 ARE SET	ADDR	CIRCUIT DECODES	GIVING
AB 7 6 5 4 3 2 1 0 0 0 0 0 X X X X	ox	AB7,6,5,4 S2,M1B-N	CSDMA-N
AB 7 6 5 4 3 2 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1	1EH 1FH	IOWRB-N ABO	CSMM-N CSFD-N
AB 7 6 5 4 3 2 1 0 0 0 0 1 0 0 0 1 0 0 0 1 0 1 0 1 0 0 0 1 0 1	11H 15H 17H 19H 1BH	AB3,2,1	CSO-N CS2-N CS3-N CS4-N CS5-N
AB 7 6 5 4 3 2 1 0 0 0 1 0 0 0 1 1 0 0 1 0 0 1 1 1 0 0 1 0 1	23H 27H 2BH	AB3,2	CS8-N CS9-N CSA-N

ABO, AB1 are hard wired to the device.

Detailed Description and Servicing Mainboard - I/O Decoder



3.1 Mainboard I/O Addresses

The Mainboard I/O addresses are given below:

Address	Signal	Device	Direction	
00 - 08	CSDMA-N	Intel 8257 DMA	read & write	e
09 - OF		Do not use		
10, 11	CSO-N	Trigger IC 7443 (74	LS107)	
12, 13	CS1-N	not used		
14, 15	CS2-N	8251A USART (for pr	inter) read & write	e
16, 17 18, 19	CS3-N CS4-N read: bit 0 : R bit 1 : C bit 2 : M bit 3 : E bit 4 : I bit 7 : C	SASI Control EQ /D-N ISG SY /O-N	read & write read & write rite: - - SEL-N RES-N	
1A 1B	CS5-N		read & write	
1C, 1D	CS6-N	not used		
1E	bit 0 to (Set to 0	Memory Manager bit 3 giving MM1 to for IPL ROM; set to	2 for System RAM)	
1 F	bit 4 : N bit 5 : M bit 6 : D	FDC Output Port EC 765 reset (active OTON S4EN (must be '1' to FSEL ('0' : FDC) ('1' : SASI)		
20 - 23 24 - 27	CS8-N CS9-N	CTC I CTC II	read & write read & write	
28 - 29 2A - 2B	CSA	SIO (Communication SIO (Terminal)	read & write	
2C - 2F	CSB	not used		



Detailed Description and Servicing Mainboard - Memory Manager

1 GENERAL

The memory manager is used to control the bank switching procedures:

- to switch between internal ROM and external RAM arrays and
- to switch over between internal RAM and the IPL ROM.

In all cases it is necessary, within each of the parallel storage areas, to have a common storage area kept free for possible information interchange between the blocks. An exception to this is external RAM access, where the function of the memory manager is handled by the external hardware.

The memory manager uses a 1024-Bit Bipolar Prom (256 x 4) 82 S 129.

2 BLOCK DIAGRAM

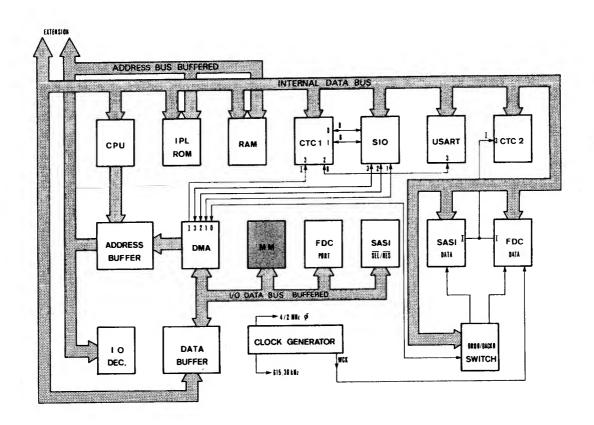


Figure 2.13 P2000C - Memory Manager Block Diagram

Detailed Description and Servicing Mainboard - Memory Manager



3 CIRCUIT DESCRIPTION

The memory manager (item 7462) is controlled by:

- two memory manager signals

 MM1 and MM2, (produced from two D-FF's 74 LS 74 item 7446)

 reachable via software with an output command to I/O address
 1EH: bit O and bit 1
- the signal EXDIS-N
- the four highest address lines.

With these signals 3 memory activities can be selected. Combinations of MM1, MM2 and EXDIS-N not shown below are not allowed:

MM2 0	MM1 0	EXDIS-N 1	address area O - 4 k	activity read from IPL ROM, write to internal RAM
0	0	1	above 4 k	internal RAM access
1	0	1	all	internal RAM access
1	1	0	all	external RAM access

Memory manager decoding is shown in table 2.14, on the following page.





Detailed Description and Servicing Mainboard - Memory Manager

Table 2.14 - Memory Manager Decoding (I)

					-				
			INP	JTS				OUTE	PUTS
HEX ADDR	MM2 (A1)	MM1 (AO)	AB15 (A2)	AB14 (A3)	AB13 (A4)	AB12 (A5)	MREQB-N (CE-N)	ROMEN-N (01)	RAMEN-N (02)
00 20 10 30 08 28 18 38 04 24 14 34 0C 2C 1C 3C	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	000000000000000000000000000000000000000	0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0	0 0 1 1 0 0 1 1 0 0 1 1 0 0 0 1 1 0 0 0 0 1	0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0 0 0 0 0
01 21 11 31 09 29 19 39 05 25 15 35 0D 2D 1D 3D	0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1	0 0 1 1 0 0 1 1 0 0 1 1 1 0 0 0 1 1 1	0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
02 22 12 32 0A 2A 1A 3A 06 26 16 36 0E 2E 1E 3E	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0	0 0 1 1 0 0 1 1 0 0 0 1 1 1 0 0 0 1 1 1	0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
03 23 13 33 0B 2B 1B 3B 07 27 17 37 0F 2F 1F 3F	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 1 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0	0 0 1 1 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0	0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0

Detailed Description and Servicing Mainboard - Memory Manager



The decoder table given in table 2.14 is repeated in table 2.15 with the addresses given in numerical order. The column DATA shows the decoder outputs (ROMEN-N, RAMEN-N) in hexadecimal.

Table 2.15 - Memory Manager Decoding (II)

ADDR	DATA	ADDR	DATA	ADDR	DATA
00	2 3	16	1	2C	1
01	3.	17	1	2D	3
02	1	18	1	2E	1
03	1	19	3	2F	1
04	1	1A	1	30	1
05	3	1B	1	31	3
06	1	1C	1	32	1
07	1	1D	3	33	1
08	1	1E	1	34	1
09	3	. 1F	1	35	3
OA	1	20	1	36	1
OB	1	21	1	37	1
OC.	1	22	1	38	1
OD	3	23	1	39	3 1
OE	1	24	1	3A	
OF	1	25	3	3B	1
10	1	26	1	3C	1
11	3	27	1	3D	3
12	1	28	1	3E	1
13	1	29	3	3F	1
14	1	2A	1		
15	3	2B	1		



Detailed Description and Servicing Mainboard - Memory Manager

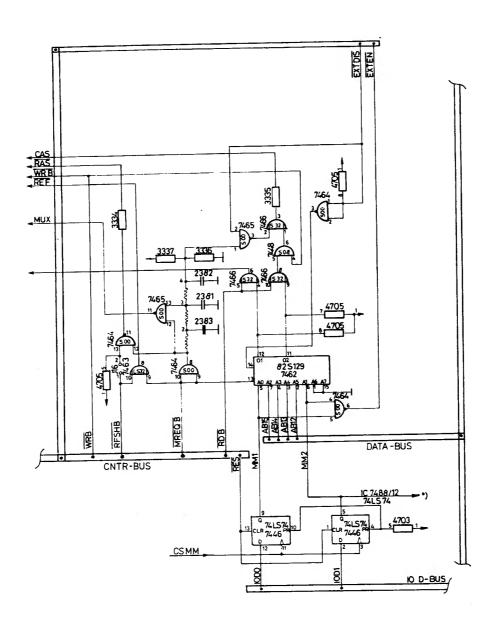


Figure 2.14 Circuit Diagram - Memory Manager

Detailed Description and Servicing Mainboard - Memory Manager



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Detailed Description and Servicing Mainboard - Random Access Memory

1 GENERAL

The P2000C Mainboard includes a 64 kByte array of HM 4864-2 random access memories. The HM 4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with double-poly N-channel silicon gate process for high performance and high functional density. It uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. In addition to the usual read, write, and read-modify-write cycles, the HM 6864 is capable of delayed write cycles, page-mode operation and RAS-N-only refresh. Full details of the HM 4864 RAM can be found in the Hitachi Data Sheets HM 4864-2 and HM 4864-3.

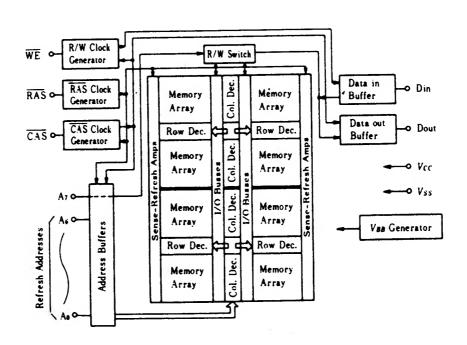


Figure 2.15 HM 4864 - Block Diagram

Detailed Description and Servicing Mainboard - Random Access Memory



2 BLOCK DIAGRAM

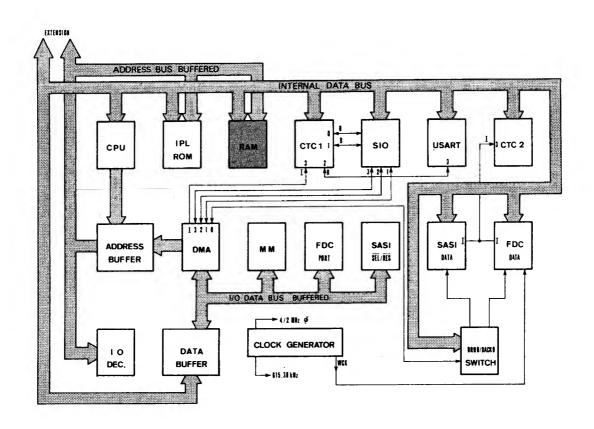


Figure 2.16 P2000C - Random Access Memory Block Diagram



3

Detailed Description and Servicing Mainboard - Random Access Memory

CIRCUIT DESCRIPTION

The RAM's (items 7478 - 7485) are addressed via the multiplexed address bus. The MUX signal (formed from MREQB-N) latches the lower 8 addresses to the dynamic RAM's. The MUX signal is formed by the first two sections of the delay line, 20 ns after the RAS-N, allowing time to write data to the RAM's. The two multiplexers 74 S 157 (items 7472/7473) are then switched over to put the higher addresses to the RAM's. On the third branch of the delay line the CAS-N signal becomes active after a further delay of about 10 ns. This signal is now gated with the output signals of the memory manager and the WRB-N and RDB-N signals. (See Memory Manager).

The WRB-N signal is used to ensure that the CAS-N signal will not be applied to the RAM's before the WRB-N signal has changed its state, as this signal becomes active very late on the Z 80. The serially arranged resistors on the multiplexer are used to avoid signal undershoot (negative voltage on the RAM inputs).

The HITACHI HM 4864-2 RAM fits into the requirements as shown below:

BASIC REQUIREMENTS						HM	486	54 − 2					
_	t	CAC	(access	time	from	CAS)	=	162	ns	maximum maximum minimum	100	ns	max max min

The refresh is done automatically by the CPU, after each Opcode fetch, using the RAS-N pulse (for the RAS-N-only refresh) derived from the MERQB-N. With the use of the HM 4864-2 RAM's, the RFSHB-N signal is not used.

At the refresh, MREQB-N will be active and both WRB-N and RDB-N will be inactive, so CAS-N will not reach the RAM's. However, the layout is designed to use RAM's with a separate refresh input (suppression of the RAS-N during refresh, RFSHB-N on the right pin).

Note: To use RAM's with separate refresh inputs, the jumpers J16 and J17 must be closed.

For situation of RAM's in relation to other Mainboard circuits, please refer to the full circuit diagrams.

Detailed Description and Servicing Mainboard - Random Access Memory



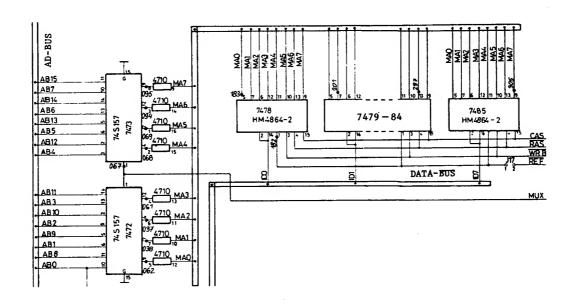


Figure 2.16a Circuit Diagram - Random Access Memory



Detailed Description and Servicing
Mainboard - IPL ROM

1 GENERAL

The basic IPL ROM used in the P2000C is a 32 k bit (4k x 8), the Intel 2732A EPROM. For special requirements it is possible to fit larger ROMs.

- 64 k bit (8k x 8 - Intel 2764-6)

- 128 k bit (16k x 8 - Intel 27128)

The IPL ROM occupies position 7456 on the Mainboard.

It should be noted that the system clock is switched from the normal 4MHz to 2MHz for the IPL operation to allow the reading of slower ROMs. As the access time for these devices is a maximum of 450ns, the access time of 525ns given by using the 2MHz system clock makes it unnecessary to use Wait Logic.

BLOCK DIAGRAM

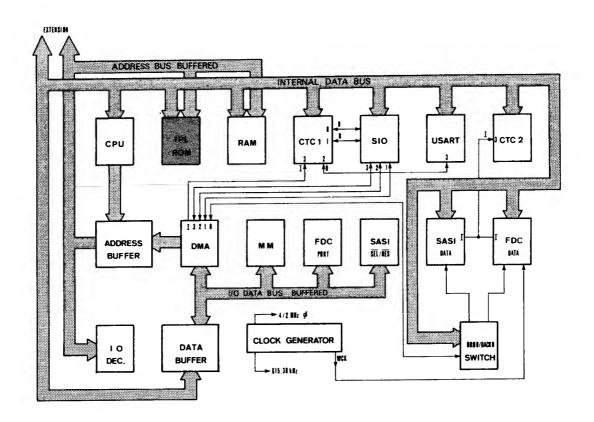


Figure 2.17 IPL ROM - Block Diagram

2

Detailed Description and Servicing Mainboard - IPL ROM



3 PINNING

The 28 pin IC socket (at item position 7456) accepts either of the larger ROMs, using all pins, and the 32 k bit ROM leaving 4 pins unused. The unused pins are 1, 2, 27 and 28, as related to the $64\ k$ bit ROM.

JUMPER J21

This jumper applies Vcc to the 32 k bit and 64 k bit ROMs in the normal position - pins 1 and 2 connected. If the 128 k bit ROM is used it is necessary to open pins 1 and 2 and to close pins 3 and 4 (input of highest address bit).

5 FUNCTION OF IPL

The purpose of the IPL (Initial Program Load) is to carry out the bootloading of the system software on switch-on (or RESET). The IPL program is first transferred to RAM and then executed. The program accesses the bootload devices in turn and, if valid 'system software' is found, transfers control information to RAM. The IPL information is overwritten at this time.

If valid data is not found the message SYSTEM DISK? is displayed. The IPL program includes a DEBUGGER program which permits basic testing of the system. The DEBUGGER can be called up by pressing the ESC key when the SYSTEM DISK? message is displayed. Details of this program are given in part 2, chapter 1 of this manual (Basic I/O System - BIOS).



Detailed Description and Servicing Mainboard - S A S Interface

1 GENERAL

The SASI (Shugart Associates Standard Interface) is an 8 bit parallel bus which is able to control a maximum of 8 devices. The main purpose of SASI is to connect computers to storage media which require an intelligent interface. (Floppy disks, Hard disks)

The SASI, as implemented on the P2000C Mainboard, does not use the full SASI specification. It is similar to the XEBEC Controller on the Hard Disk.

- Transfers can only be initiated from the Mainboard
- Only one target can be active at any time
- The Arbitration and Reselection phases are not implemented

2 BLOCK DIAGRAM

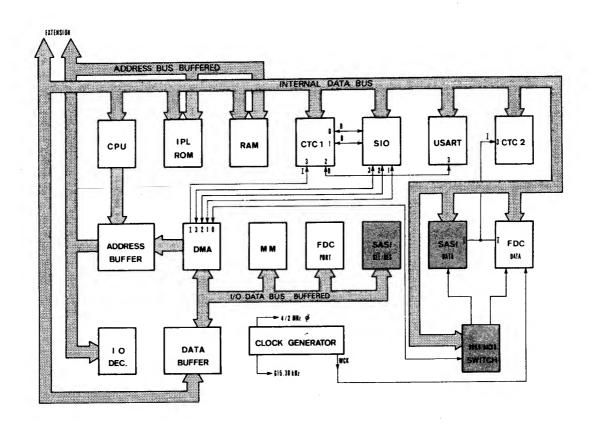


Figure 2.18 P2000C - SASI Block Diagram

3

10-2

Detailed Description and Servicing Mainboard - S A S Interface



CIRCUIT DESCRIPTION

3.1 Description of a Data Transfer

CPU TRANSFER

After the establishment of the path between the Initiator (Mainboard) and the Target (storage controller) and the transfer of the necessary control data (data address, block length, direction of transfer) the data transfer starts. The Target announces a data request (REQ = "1", C/D-N = "0"), releasing D-FF (Item 7429-1) from the clear state. In polled mode, the CPU acknowledges the Request state and then sends or reads data.

DMA TRANSFER

The 74 LS 156 decoder (item 7530) recognizes the request state because of the state of lines REQ and C/D-N and sets the D-FF (Item 7429-2). The Q output of the D-FF (Item 7429-1) gives the DRQ (Data Request) signal for the DMA Chip which, in turn, initiates the corresponding write or read command.

IN BOTH CASES (CPU/DMA)

The data read or write procedure leads to an active signal on the clear input of D-FF (Item 7429-1) (ACK-N is activated and informs the target that the information is ready to be fetched or that it has arrived.)

After a time the target cancels the REQ line and the D-FF (Item 7429-1) will be reset (ACK-N will be inactive again). If an error occurs during the transfer the target is able to give a message (or a Status byte) to the Initiator. The 74 LS 156 Decoder recognizes such a state on the SASI control bus and generates an interrupt by using the CTC II Channel 3. The CTC II Channel 3 is used by both the SASI and the Floppy Disk Controller. It is the responsibility of the software to interpret the interrupt correctly.



Detailed Description and Servicing Mainboard - S A S Interface

Note: SASI or FDC are selected by software via FDC output port using the SFSEL signal, both using the DMA channel 0. The FDC output port address is 1FH; bit 7 set to 1 means SASI active and FDC inactive.

If SASI is selected, it is important that the FDC is reset by software to ensure that the DRQ FDC does not become active .

If FDC is selected, the SFSEL signal ensures that the DRQ SASI does not become active, by setting D-FF (Item 7429-2) clear input.

An OR-gate (IC 7426, pins 11, 12 and 13) combines the two DRQ signals from SASI and FDC to produce one DRQO signal for the DMA chip.

Item 7410 (74 LS 240) is an inverting bus driver so, for example, C=N/D on the input corresponds to C/D=N on the output.

3.2 Driver Current Requirements

All lines of the SASI bus (excluding ACK-N, SEL-N and RES-N) must be terminated with 220 0hm/330 0hm resistor networks at each end, to prevent reflections (Item 4702 on the P2000C Mainboard). Each line has to be able to drive 7 Shottky components. In the case of the P2000C version of the SASI, the lines ACK-N, SEL-N and RES-N are used as outputs only and must be terminated (on the receiver side only) with a network having a value equal to the surge impedance. (LS components can now be used). The circuit arrangement is shown in figure 2.19.

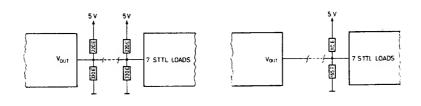


Figure 2.19 P2000C - SASI Line Terminators

Detailed Description and Servicing Mainboard - S A S Interface



3.3 Control

The control ports (Input & Output) are accessed by the CPU with an I/O command. The data ports can be accessed with an I/O command by the CPU and also by the 8257 DMA. Because of this a fast data transfer to and from the storage media is possible.

3.4 I/O Addresses

16 or 17	CS3-N	SASI Data	read & write
18 or 19	CS4-N	SASI Control	read & write

read:	write:
bit 0 : REQ	only bit 2 and 3
bit 1 : C/D-N	used
bit 2 : MSG	bit 2 : SEL
bit 3 : BSY	bit 3 : RES
bit 4 : I/O-N	
bit 5 : not used	
bit 6 : not used	
bit 7 : C/D-N	

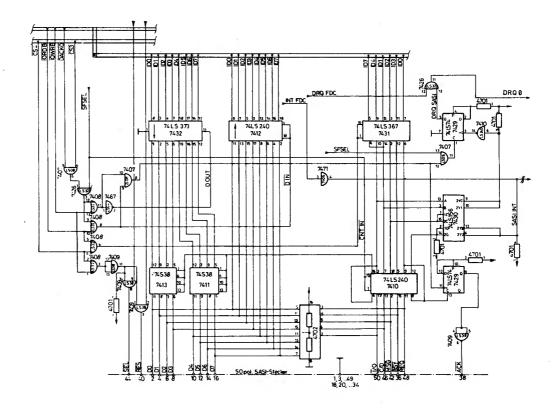


Figure 2.20 Circuit Diagram - SASI



Detailed Description and Servicing Mainboard - Flexible Disk Controller

1 GENERAL

1.1 uPD 765 Disk Controller - General

The uPD 765 is an LSI Floppy Disk Controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The uPD 765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface. Figure 2.21 shows the main functions.

Full details of the uPD 765 can be found in the NEC Microcomputers Inc. Data Sheet.

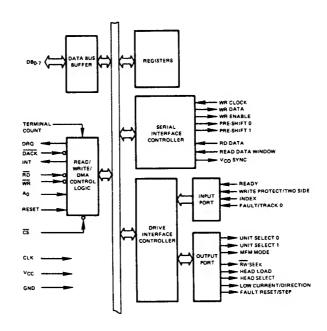


Figure 2.21 P2000C - FDC Block Diagram

Detailed Description and Servicing Mainboard - Flexible Disk Controller



1.2 Application in P2000C

The flexible disk controller is designed to handle up to four single/double sided - single/double density - 5½" flexible disk drives. See NEC Application Note 10 for the uPD 765.

1.3 Flexible Disk Controller Technology

The flexible disk controller, uPD 765, provides control over the following functions:

- disk formatting
- recalibration of head on track 0
- seeking specified track
- writing n sectors
- reading/writing deleted data
- scanning (comparing two disks track by track)
- software selectable data format and drive parameters

2 BLOCK DIAGRAM

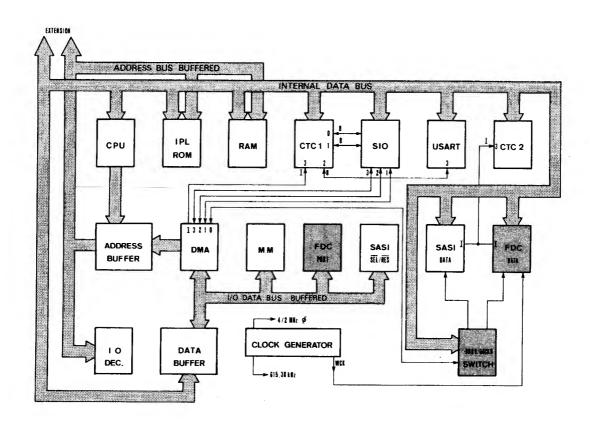


Figure 2.22 P2000C - FDC Block Diagram



3

Detailed Description and Servicing Mainboard - Flexible Disk Controller

CIRCUIT DESCRIPTION

The data separator, PLL, performs the following functions:

- high quality data recovery

- an 8257 DMA chip controls access to and from RAM memory. (A bus request is given to the CPU before a memory transfer is required. The disk control unit DMA is then enabled by the CPU and controls memory accessing, thus allowing the CPU to proceed with other activities.)

improvements have been made to the following Note: application circuit shown in NEC Application Note number 10:

- the current source (Q2 2N2222) used for adjusting the middle frequency of the VCO MC 4024 P (item 7417) has been replaced by a temperature compensated current source, consisting of two BC 549's (items 7302/7303). The frequency can be adjusted by using the potentiometer, item number 4712, detailed in paragraph 3.4. Full details of the MC 4024 P can be found in the Motorola Data Sheet for the device.
- to improve mid-frequency stability when no data is being received, some circuitry has been added. The 250 kHz signal, from the system clock, is fed to the PLL circuit via a multiplexer IC 7420 (4 x 74 LS 00). This signal replaces the data signal, ensuring that feedback is available in the closed control loop to prevent VCO frequency drift. The switch over of the signals is made by the VCO Sync signal from the uPD 765.

3.1 Integrated Circuits

IC 74 LS 244 - Item 7454 Additional explanation is neccessary for this component. It is used as a demultiplexer and is controlled by the RW-N/SEEK signal. Two of the four leads are inputs, the other two are outputs. They have functions both in the R/W mode and in the SEEK mode. The STEP bus driver is also controlled by the RW-N/SEEK signal, to avoid faulty stepping during the switch over of the signal. This faulty stepping will also occur if the 74 LS 244 goes to the tri-state mode, because in this case the STEP line becomes 0.

Detailed Description and Servicing Mainboard - Flexible Disk Controller



IC 74 LS 175 - Item 7452 FDC Output Port
This 4 bit output port (I/O address 1FH write only) is software controlled and fulfils 4 functions:

bit 4: a logic "O" resets the NEC 765 FDC

bit 5: "motor on" signal

bit 6: drive select enable; must be "1" to address drive 4

Note: Two outputs are implemented in the FDC for selecting 4 drives. If no drive is addressed both outputs are high, thus selecting drive 4, and the select LED of this drive is permanently active although the drive is not accessed. The drive 4 select enable signal is for inhibiting this unwanted mode.

bit 7: SFSEL "0" FDC active
"1" SASI active

FDC and SASI use the same DMA channel (channel 0) and the same interrupt input on the CTC II (channel 3). With this control bit the system software determines the source/target of data transfer or interrupt. The unused function must always be inactive.

3.2 Flexible Disk Controller Hardware Interface

The flexible disk controller connections to the $5\frac{1}{4}$ " flexible disk drive are via a 34-pin connector and are as follows:

PIN	PURPOSE
2	spare
4	head load/in use
6	drive select 4
8	index
10	drive select l
12	drive select 2
14	drive select 3
16	motor on
18	direction
20	step
22	write data
24	write gate
26	track 0
28	write protect
30	read data
32	side select
34	ready
	•

Pins 1,3,5,...33 are connected to ground.



Detailed Description and Servicing Mainboard - Flexible Disk Controller

Flexible Disk Controller Software Interface (I/O Ports)

The standard addresses for I/O devices are:

PORT	USAGE
1AH,1BH	Read/write output port
	_
1FH	CS FDP write only
	bit 4 FDC RESET
	bit 5 MOTON
	bit 6 DS4EN
	bit 7 SFSEL: 0 = FDC
	1 = SASI

3.4 Adjustment of VCO Middle Frequency

The following procedure should be used to adjust the VCO middle frequency:

- apply power to the Mainboard
- connect pin 3 of item 7415 (IC 74 LS 221) to ground
- measure the frequency on TP2 (using a frequency counter)
- adjust the frequency to 500 kHz \pm 1-1% using the potentiometer item 4712

The monoflop should then be adjusted as follows:

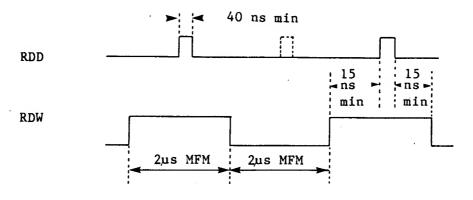
- remove the connection between pin 3 of item 7415 and ground
- examine the waveform on TP1 (using an oscilloscope)
- measure the time between falling and rising edges of the waveform
- adjust the time to as near as possible to 1 microsecond using the potentiometer item $4713\,$

11-6

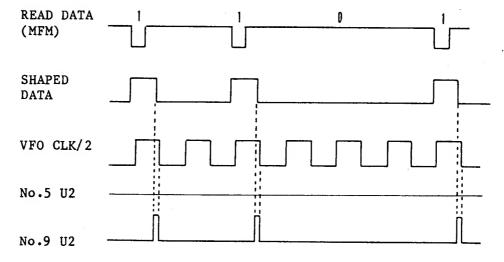
Detailed Description and Servicing Mainboard - Flexible Disk Controller



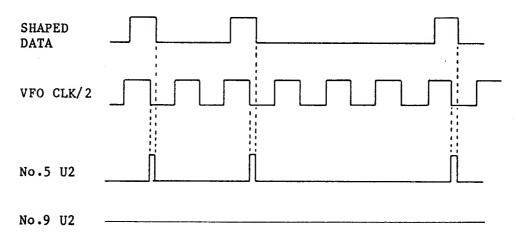
4 TIMING DIAGRAMS



Input Data Timing



Phase Detector - CLK Lagging Shaped Data



Phase Detector - CLK Leading Shaped Data

Figure 2.23 - FDC Timing Diagram



Detailed Description and Servicing Mainboard - Flexible Disk Controller

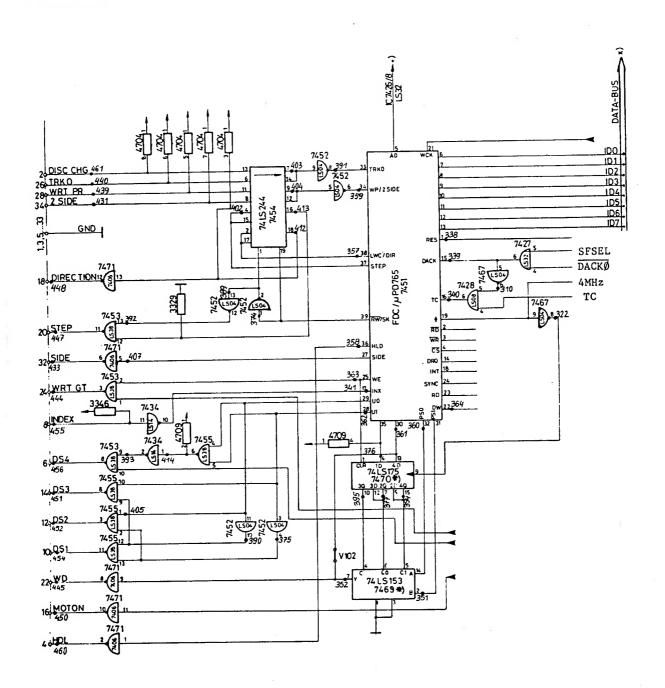


Figure 2.24 Circuit Diagram - Flexible Disk Controller

Detailed Description and Servicing Mainboard - Flexible Disk Controller



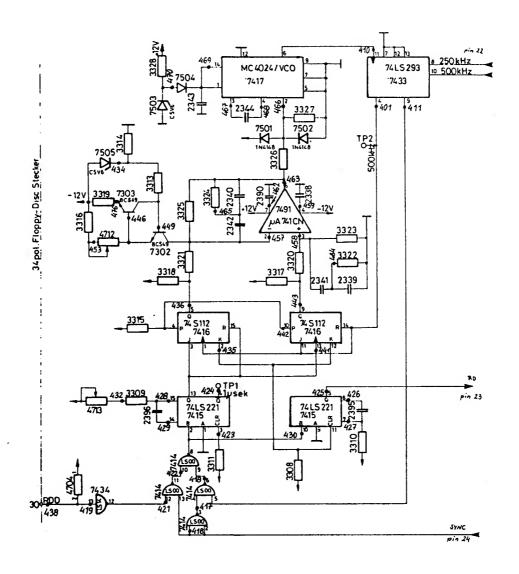


Figure 2.24 Circuit Diagram - Flexible Disk Controller (PLL)



Detailed Description and Servicing Mainboard - Baud Rate Generator - C T C

1 GENERAL

The P2000C uses two Z80A CTC Counter/Timer Circuits (Z8430A). The main features of the Z80A CTC are:

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Three channels have Zero Count/Time Out outputs capable of driving Darlington transistors.
- Selectable positive or negative trigger initiates time operation.
- Standard Z80 Family daisy-chain interrupt structure provides fully vectored interrupts (with priority levels) without external logic. The CTC may also be used as an interrupt controller.
- Interfaces directly to the Z80 CPU or to the Z80 SIO for baudrate generation.

Full details of the Z80A CTC can be found in the Z8430A Product Specification.

The CTC has four major elements, as shown in figure 2.24

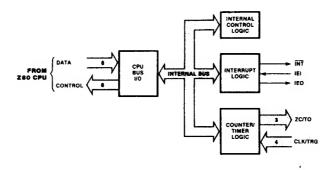


Figure 2.25 Z80A CTC - Block Diagram

Detailed Description and Servicing Mainboard - Baud Rate Generator - C T C



2 BLOCK DIAGRAM

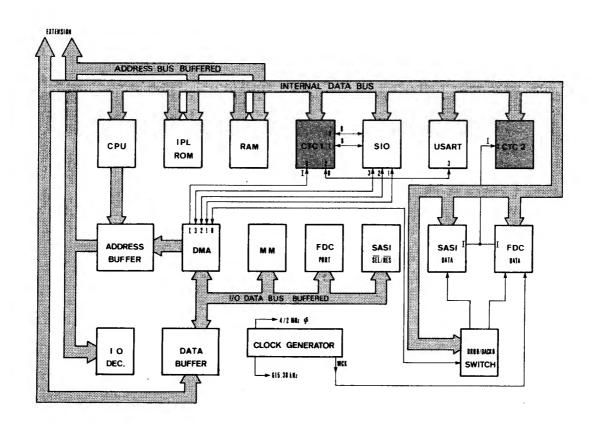


Figure 2.26 P2000C - CTC Block Diagram



Detailed Description and Servicing Mainboard - Baud Rate Generator - C T C

3 CIRCUIT DESCRIPTION

The CTC's in the P2000C are used both as baudrate generators and interrupt controllers for the system timer and for non-Z80 devices.

3.1 CTC 1

CTC 1 (item 7449) modifies the input signal (615.38 KHz) to produce the signals 'TCO' and 'TC1' which are divided by 2 in the D-flip flops (item 7447), resulting in ASYNO and ASYN2. ASYN 1 is a direct output.

3.2 CTC 2

Channel 2 of CTC 2 (item 7450) is used to monitor an external interrupt on the bus extension connector or for baudrate signal generation (ASYN3). A jumper (J15) is used to determine the function of this channel. (Pins 2 & 3 normally connected). Channels 0 and 1 of CTC 2 (item 7450) are cascaded and can be used as the system clock or clock/timer by the BIOS. The output of channel 0 is connected to an optional connector (PC), giving the possibility of a simple sound source.

CTC 1 INPUTS & OUTPUTS

	I/O				OUTPUT
	ADD	INPUT	OUTPUT	REMARKS	SIGNAL
Ch.0	20H	CLK	ZC/TOO	/2 (D-FF)	= ASYNO
Ch.1	21H	CLK	ZC/TO1		= ASYN1
Ch.2	22H	CLK	ZC/TO2	/2 (D-FF)	= ASYN2
Ch.3	23H	TC	-	DMA INT	

CTC 2 INPUTS & OUTPUTS

	I/O ADD	INPUT	OUTPUT	REMARKS	OUTPUT SIGNAL
Ch.0 Ch.1 Ch.2	24H 25H 26H	ZC/TO1 CLK ZC/TO1-	ZC/TOO ZC/TO1	PC (sound) CLO & CL2	
Ch.3	27Н	E INT TC	ZC/TO2 -	SASI/FDC INT	= ASYN3

Detailed Description and Servicing Mainboard - Baud Rate Generator - C T C



3.3 Baud Rate Relationships

The relationships between the system clock, scaling factors and final baud rates are shown in the following tables. The shading shows an example of the use of the tables.

	SIO	Clock	Mode
Baud Rate	x16	x32	x64
75	11111	2,400	4,800
150	2,400	4,800	9,600
300	4,800	9,600	19,200
600	9,600	19,200	38,400
1200	19,200	38,400	76,800
2400	38,400	76,800	153,600
4800	76,800	153,600	307,200
9600	153,600	307,200	614,400
19200	307,200	614,400	//////

CTC Time Constant

	ASYN1	ASYN3	ASYN2
Clock Speed	21H	26H	22H
2,400	0	0	7///
4,800	128	128	0
9,600	64	64	128
19,200	32	32	64
38,400	16	16	32
76,800	8	8	16
153,600	4	4	8
307,200	2	2	4
614,400	1	1	2





Detailed Description and Servicing Mainboard - Baud Rate Generator - C T C

A summary of the Z80A CTC programming is shown in figure 2.26. Full details of the CTC can be found in the Z8430 Z80A CTC Product Specification.

CTC CHANNEL INTERRUPTS WHEN 01H IS DECREMENTED TO OOH

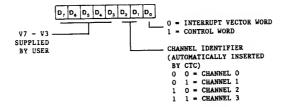
T IME CONSTANT	DECIMAL COUNTS TO INTERRUPT
01H	1
	•
	•
FFH	255
оон	256

REGISTER SELECTION

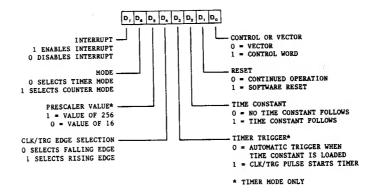
SELECT CS1	LINES CSO	CHANNEL SELECTED	PRIORITY
0	0	0	HIGHEST
0	1	1	1
1	0	2	
1	1	3	LOWEST

READ = DOWN COUNTER WRITE = CONTROL REGISTER

Interrupt Vector Word



Channel Control Word



Time Constant Word

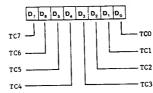


Figure 2.27 CTC Programming

Detailed Description and Servicing Mainboard - Baud Rate Generator - C T C



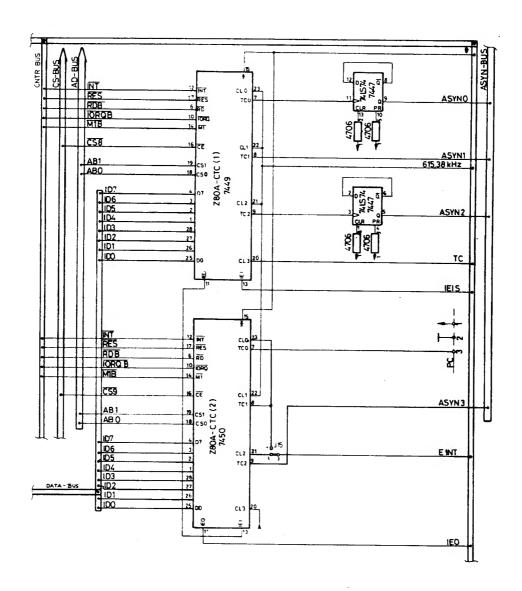


Figure 2.28 Circuit Diagram - CTC



Detailed Description and Servicing Mainboard - Serial Interfaces

1 GENERAL

There are three fully duplexed serial channels.

- a) Terminal Interface
- b) Communication Interface
- c) Printer Interface
- a) and b) are controlled by a Z80A SIO
- c) is controlled by an 8251 USART

1.1 Z80A SIO - Z8440

The P2000C uses a Z80A SIO Serial Input/Output controller. The main features of the Z80A SIO are:

- two independent full-duplex channels, with seperate control and status lines for modems or other devices.
- data rates of 0 to 800 Kbits per second, with a 4 MHz clock.
- asynchronous protocols: capable of handling complete messages in 5, 6, 7 or 8 bits per character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; and overrun and framing error detection.
- synchronous protocols: capable of handling complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits per character, including IBM Bisync, SDLC, HDLC, CCITT-X-25 and others. Includes automatic CRC generation/checking; sync character and zero insertion/deletion; abort generation/detection and flag insertion.
- receiver data registers quadruply buffered, transmitter registers doubly buffered.
- highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

Detailed Description and Servicing Mainboard - Serial Interfaces

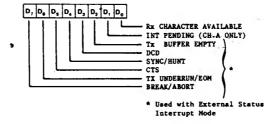


SIO Registers

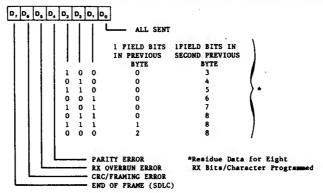
Channel Selection

C/D	B/A	FUNCTION
0	0	CHANNEL A DATA
0	1	CHANNEL B DATA
1	0	CHANNEL A COMMANDS/STATUS
1	1	CHANNEL B COMMANDS/STATUS

Read Register 0



Read Register 1 (Used with Special Receive Condition Mode)



Read Register 2

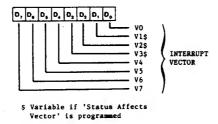


Figure 2.29 SIO Programming - Read Registers



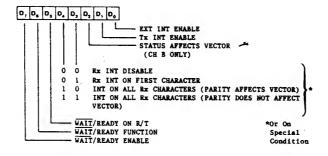


Detailed Description and Servicing Mainboard - Serial Interfaces

Write Register 0

$\boxed{\textbf{D}, \left[\textbf{D}_{4} \mid \textbf{D}_{5} \mid \textbf{D}_{4} \mid \textbf{D}_{7} \mid \textbf{D}_{2} \mid \textbf{D}, \mid \textbf{D}_{0}\right]}$
I O O O REGISTER O
0 0 1 REGISTER 1
0 1 0 REGISTER 2
0 1 1 REGISTER 3
1 0 0 REGISTER 4
1 0 1 REGISTER 5
1 1 0 REGISTER 6
1 1 1 REGISTER 7
0 0 0 NULL CODE
0 0 1 SEND ABORT (SDLC)
0 1 0 RESET EXT/STATUS INTERRUPTS
0 1 1 CHANNEL RESET
1 0 0 ENABLE INT ON NEXT Rx CHARACTER
1 0 1 RESET Tx INT PENDING
1 1 0 ERROR RESET
1 1 1 RETURN FROM INT (CH A ONLY)
0 0 NULL CODE
0 1 RESET Rx CRC CHECKER
1 0 RESET Tx CRC GENERATOR
1 1 RESET Tx UNDERRUN/EOM LATCH

Write Register 1



Status Affects Vector (D2 from WR1)

	V3	V2	V1	
	0	0	0	CH B TRANSMIT BUFFER EMPTY
	0	0	1	CH B EXTERNAL STATUS CHANGE
CHANNEL B	0	1	0	CH B RECEIVE CHARACTER AVAILABLE
	0	-1	1	CH B SPECIAL CONDITION
	0	0	0	CH A TRANSMIT BUFFER EMPTY
CHANNEL A	0	0	1	CH A EXTERNAL STATUS CHANGE
	0	1	0	CH A RECEIVE CHARACTER AVAILABLE
	0	1	1	CH A SPECIAL CONDITION

If this mode is selected, the vector returned from an Interrupt Acknowledge Cycle will be according to this table. If this bit is 0, the fixed vector programmed in the Vector Register is returned.

Figure 2.30(i) SIO Programming - Write Registers

Detailed Description and Servicing Mainboard - Serial Interfaces



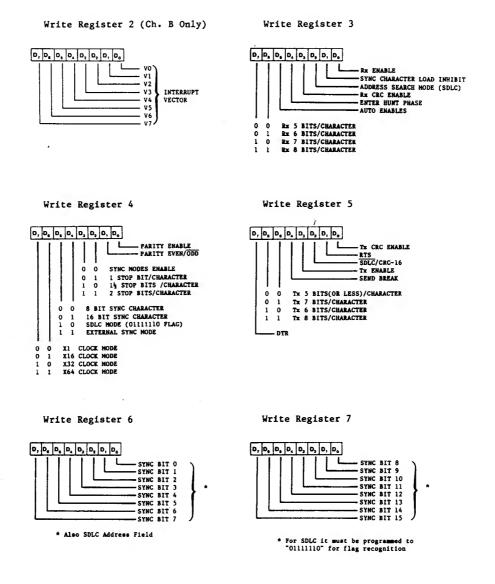


Figure 2.30(ii) SIO Programming - Write Registers



Detailed Description and Servicing Mainboard - Serial Interfaces

1.2 USART - 8251A

The P2000C uses an Intel 8251A as controller for the printer interface, as shown in figure 2.31. The main features of the 8251A USART are:

- the 8251A has double-buffered data paths with seperate I/O registers for control, status, Data In and Data Out. This simplifies control programming and minimizes CPU overhead.
- in asynchronous operations the receiver detects and handles 'break' automatically, relieving the CPU of this task.
- a refined Rx initialization procedure prevents the receiver from starting when in the 'break' state, thus suppressing unwanted interrupts from a disconnected USART.
- Tx Enable logic enhancement prevents a Tx disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- synchronous baud rate from DC to 64K

Full details of the 8251A USART can be found in the Intel 8251A/S2657 Data Sheet.

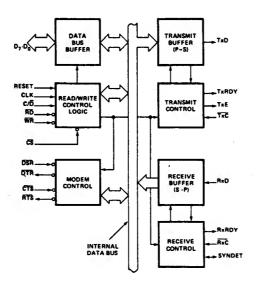


Figure 2.31 8251A USART - Block Diagram

Detailed Description and Servicing Mainboard - Serial Interfaces



2 BLOCK DIAGRAM

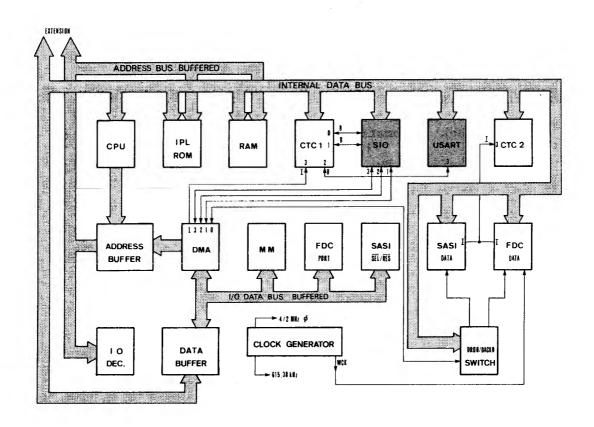


Figure 2.32 P2000C - Serial Interfaces Block Diagram



Detailed Description and Servicing Mainboard - Serial Interfaces

3 CIRCUIT DESCRIPTIONS

3.1 General

The P2000C has three fully duplexed serial channels:

- a) Terminal Interface
- b) Communication Interface
- c) Printer Interface
- a) and b) are controlled by the Z80 A SIO
- c) is controlled by the 8251 USART

The transmit data of the Terminal interface (Video out) and the transmit and receive data of the communication interface can be moved to and from the SIO with CPU I/O commands or with DMA (Direct Memory Access).

It is possible for the SIO to initiate an interrupt.

The printer interface is used without interrupt and without DMA.

The SIO and the USART are able to work synchronously or asynchronously. Complicated synchronous protocols (e.g. SDLC and HDLC) can only be handled with the SIO.

3.2 Baudrate Selection

All serial channels can be supplied by the internal baudrate generators (CTC's). The real baudrate is calculated as follows:

FBd =	6	15380	
1	tCTC x	tFF x	tUSART

where:		
FBd	=	clock frequency in Hz
615380	=	basic frequency, in Hz. All other clocks are derived from it.
tCTC	=	division factor of the particular CTC channel
tFF	=	division factor of 2 or 1, depending on whether or not a flip-flop is added to the CTC channel, for forming the duty cycle. tFF = 2 for terminal interface tFF = 1 for communication interface
tUSART	=	internal division factor of 1,16 or 64 in the USART or SIO, and is selectable by software.

Detailed Description and Servicing Mainboard - Serial Interfaces



Example: The printer interface is required to work at 19200 Bd.

With: tCTC = 1 tFF = 2 tUSART=16

1	FBd	=		61	538	Ō		=	19230	=	19200 + 0.16%
1			1	x	2	x	16				

Because of the internal circuits of the SIO and the USART the tUSART should not be 1, to ensure correct operation. (The only exception is the communication interface when used in a synchronous mode and with an external clock).

3.2.1 MAXIMUM BAUDRATES

The maximum baudrates for the P2000C Serial Interfaces are as follows:

- For the terminal and the printer interfaces 19,200 Bd
- For the communication interface

(internally clocked)38,400 Bd(externally clocked)500,000 Bd

(500,000 Bd is the limit given in the SIO data sheet. As the SIO clock is switched between 4 and 2 MHz baudrates, limit calculations must be made using the 2 MHz value.)

3.3 Terminal Interface

The terminal interface is controlled by the SIO (item 7441), channel B. (I/O Address 28H - 2BH).

Transmit data (video output) also can be sent via DMA Channel3. (W/RDYB-N must be programmed for transmit data). Receive data (keyboard input) will be fetched only by CPU.

When using an external terminal, the internal terminal must be disconnected. If optional drivers (items 7406/7404) are fitted in assemblies with PRINT number up to .2 (ASSY No up to .1) (see 3.1 0-2) the print tracks between driver and SIO must be cut (pins 3, 6 & 8) to avoid signal conflict if the internal terminal is used. When using synchronous modems the drivers must be fitted. A gate of item 7404 is used for the DSR signal.



Detailed Description and Servicing Mainboard - Serial Interfaces

3.3.1 BAUDRATE GENERATOR

The terminal baudrate generator is CTC 1 (Item 7449). Channel 0 output TCO is used, via D-FF (Item 7447-2), to produce ASYN 0. (tFF = 2)

Note: An external clock can also be used from the terminal board, via a jumper.

3.4 Communication Interface

It is controlled by the SIO (item 7441) channel A. (I/O address 28H - 2BH). 22 3.2 6-4 (20H)

There is only one W/RDYA-N output available for controlling channel A of the SIO. To control both channels (transmit and receive) via DMA the following actions are carried out:

One SIO channel is directly connected to the DMA via W/RDYA-N (DMA channel 2). As soon as the other SIO channel (e.g., transmit data) issues an interrupt, which indicates that a data transfer is neccessary, the CPU sets an I/O write to address 10H or 11H during the interrupt routine. A flip-flop is then set, demanding the DMA channel 1 to do a data transfer. The DMA chip must be correctly programmed beforehand.

Which DMA channel (1 or 2) handles transmitted or received data depends on the programming of the SIO and the DMA.

3.4.1 BAUDRATE GENERATOR

Transmitter Clock

The communication transmitter uses ECLK1 - PSE 2 pin 15. This signal is normally supported by a synchronous modem

Receiver Clock

The communication receiver uses ECLK2 - PSE 2 pin 17. This signal is also supported by a synchronous modem.

Detailed Description and Servicing Mainboard - Serial Interfaces



Note: Nearly all combinations of clock signals (two External Clock connections, ASYN 3 or ASYN 1) are possible on the transmitter and receiver clock inputs, using jumpers J10, J12 and J13. Full details are shown in table 2.16.

To use the Communications channel in an asynchronous mode, connect ECLKO (PSE 2 pin 24) to ECLK1 & 2 (PSE 2 pins 15 & 17). In this case Baud rate generator ASYN1 determines the clock frequency for both the receiver and the transmitter.

Channel 2 of CTC 2 is used for external interrupt input for IEEE (P2012), but can be used to produce ASYN 3.

3.4.2 JUMPER J 20

This jumper routes the DSR (data set ready) signal to the SYNC inputs of the SIO. The normal condition is with pins 2-4 & 3-4 short circuited, routing DSR to the SYNCB input of the SIO.

3.5 Printer Interface

The printer interface is controlled by the USART. (1/0 address 14H - 15H).

On this interface it is not possible to give an interrupt or to work through DMA.

3.5.1 BAUDRATE GENERATOR

The printer interface uses CTC 1 (Item 7449) for both the transmitter and receiver clocks. Channel 2 output TC2 is used, via D-FF (Item 7447-1), to produce ASYN 2. (tFF = 2)



Detailed Description and Servicing Mainboard - Serial Interfaces

3.6 Connection - Mainboard to Terminalboard

As the connection between the Mainboard and the Terminalboard is internal to the P2000C cabinet, the RS 232 drivers and receivers can be omitted and the system will work directly at TTL levels. If the Mainboard is used with an external terminal or the Terminalboard used as a stand alone terminal, the RS 232 components and the D-device plug can be implemented.

3.7 Jumpers

3.7.1 D-DEVICE PLUGS

The pin allocation on devices used with the P2000C may differ. To avoid the necessity of cross over of external cables, all logical signal pairs on the D-device plugs are reversible by jumper. These signal pairs are:

RxD - TxD CTS - RTS DTR - DSR

The jumpers involved are J1 through J9 and full details of their use are given in table 2.16. Connections marked "*" represent the standard setting as shown in figure 2.33. Pin 1 of the connectors PSE1, PSE2 and PSE3 are connected to the connector housing.

3.7.2 BAUDRATE SELECTION

Clock selection for channels A & B of the SIO is controlled by jumpers J1O through J13. The standard configuration of these four jumpers gives the following baudrate selections, where channel A is connected as for a Standard Synchronous Modem:

Channel A TxC = ECLK 1
Channel A RxC = ECLK 2 (J12 = 3 - 4 / J10 = 1 - 2)
Channel B RxTxC = ASYN 0 (J11 = 1 - 3)

Full details of the baudrate clock selection jumpers are given in table 2.16. Connections marked "*" represent the standard setting as shown in figure 2.33.

Detailed Description and Servicing Mainboard - Serial Interfaces



Table 2.16 - Serial Interface Jumpers

PRINTER CONNECTOR (PSE 3)

	J1			J2			J3	
PIN	RxD	ΤxD	PIN	CTS	RTS	PIN	DSR	DTR
2	3-4*	2-4	4	5-6	4-6	6	4-2	1-2*
3	3-1	2-1*	5	5-3	4-3*	20	4-3*	1-3
			perm	1-2*	_			
			(pin	2 to	+12V)			

COMMUNICATION CONNECTOR (PSE 2)

	J4			J5			J6	
PIN	RxD	TxD	PIN	CTS	RTS	PIN	DCD	DTR
2	3-4	2-4*	4	5-6	4-6*	8	4-2*	1-2
3	3-1*	2-1	5	5-3*	4-3	20	4-3	1-3*
			(see	note	below)			

TERMINAL CONNECTOR (PSE 1)

	J7			J8			J9	
PIN	RxD	TxD	PIN	CTS	RTS	PIN	DSR	DTR
2	3-4*	2-4	4	5-6*	4-6	6	4-2	1-2*
3	3-1	2-1*	5	5-3	4-3*	20	4-3*	1-3
			(see	note	below)			

Notes: 1) A permanent CTS can be arranged by routing +12V (on pin 1) to pin 5, via the jumpers.

2) The connector PSE 1 is not fitted to the board.

BAUDRATE SELECTION

	TxC A	RxC A	RxTxC B
ASYN 1	J13/1-2	J13/1-2 J12/1-3	
ASYN 3	not possible	J12/5-3	
EXT 1 PIN 15	J12/1-2*	J12/2-4 & 3-4	
EXT 2 PIN 17	J10/1-2	J10/1-2*	
	J12/4-3 & 3-1	J12/4-3*	
EXT 3 PIN 25	(see note below)		
ASYN O			J11/1-3*
TERM BOARD			J11/2-3

Note: In the new layout for the Mainboard, ASYN 3 is routed to pin 25 of PSE 2 as EXT 3. It is therefore possible to drive transmitter and receiver at different baud rates for asynchronous operation via pins 15 (Tx) and 17 (Rx) of PSE 2.



Detailed Description and Servicing Mainboard - Serial Interfaces

3.7.3 JUMPERS - PHYSICAL CONNECTIONS

Figure 2.33 shows the physical connections for the standard settings of the serial interface jumpers. The pin numbering convention, as used in any drawings or diagrams, is shown. These numbers do not appear on the printed circuit board.

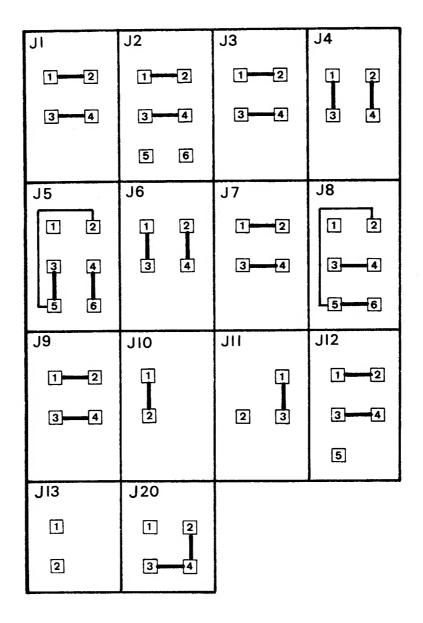


Figure 2.33 Serial Interface Jumpers

Detailed Description and Servicing Mainboard - Serial Interfaces



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Detailed Description and Servicing

Mainboard - Bus Extension

1 **GENERAL**

It is possible to extend the capabilities of the P2000C with the use of one additional board. On the Mainboard, buffered outputs are available via a 120 way connector. The bi-directional data bus allows one low power shottky load (50pF). Pin connections for the Bus Extension are shown in table 2.17.

Table 2.17 - Bus Extension

	PIN	SIGNAL	DIRECTION		PIN	SIGNAL	DIRECTION
	01	8 MHz B	OUT		53	TODOD_N	OUT
-	03	CLOCK	OUT		55	IORQB-N AB15	OUT
•							
	05	2 MHz B	OUT		57	AB14	OUT
	07	EXTEN-N	OUT		59	AB13	OUT
	09	EXTDIS-N	IN		61	AB12	OUT
	11	NC	-		63	AB11	OUT
	13	EINT-N	IN		65	AB10	OUT
	15	NC .	-		67	AB9	OUT
	17	NC	_		69	AB8	OUT
	19	HALTB-N	IN		71	AB7	OUT
	21	WAIT-N	IN		73	AB6	OUT
	23	RESET-N	IN		75	AB5	OUT
	25	NMI-N	IN		77	AB4	OUT
PR /	27	INT-N	IN		79	AB3	OUT
	29	NC	-		81	AB2	OUT
-	31	IEO-N	OUT		83	AB1	OUT
	33	NC	-		85	ABO	OUT
	35	BAO-N	OUT		87	D7	IN/OUT
	37	NC	_		89	D6	IN/OUT
	39	BUSAK-N	OUT		91	D5	IN/OUT
	41	BUSRQ-N	IN		93	D4	IN/OUT
	43	WRB-N	OUT		95	D3	IN/OUT
	45	RDB-N	OUT		97	D2	IN/OUT
	47	RFSHB-N	OUT		99	D1	IN/OUT
-	49	M1 B-N	OUT		101	DO	IN/OUT
	51	MREQB-N	OUT				•
		•					
	Pins	107 - 110	-12 V				
	Pins	113 - 116	+12 V				
	Pins	117 - 120	+ 5 V				
	Pins	2, 4, 6	106, 103,	105, 111	& 112	- GND	

Detailed Description and Servicing Mainboard - Bus Extension



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Detailed Description and Servicing Terminalboard - Introduction

1 GENERAL

The Terminalboard, which is connected to the Mainboard by a serial interface (USART 8251 A), carries out the following functions:

- control of a b/w monitor
- scanning of the keyboard
- control of the beeper

The CPU and CRTC work synchronously to ensure a rapid update of the screen image. Controlled by the character clock, the CPU and CRTC manage the address bus and the data bus alternately. The CPU has unlimited access to the video refresh RAM, without disturbing the video image (Interleaving mode).

Two banks with 16 kByte RAM and 8 kByte ROM are reserved for storage.

There are three different kinds of image representation:

- alphanumeric with 5 attributes
- medium resolution graphics in 4 grey shades, with alphanumeric representation
- high resolution graphics with alphanumeric representation

Some functions (graphic, keyboard, attribute treatment) can be controlled via an I/O port. The keyboard is scanned by video refresh addresses and, if a key is depressed, it gives a strobe to the light pen input of the CRTC. The decoded key address is stored in the light pen register. The Terminalboard can also be used as an independent data terminal (with graphics) by the use of an optional V24 interface.

Detailed Description and Servicing Terminalboard - Introduction



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Detailed Description and Servicing Terminalboard - CPU

1 GENERAL

This is the same device as used on the Mainboard and general comments dealing with the Z80 CPU can be found in that section.

2 BLOCK DIAGRAM

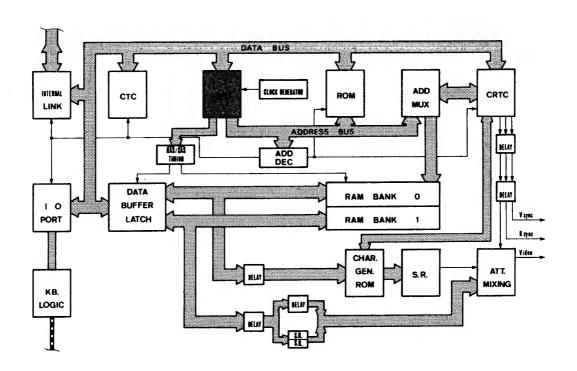


Figure 3.1 P2000C - CPU Block Diagram

Detailed Description and Servicing Terminalboard - CPU



3 CIRCUIT DESCRIPTION

The Z80A CPU (item 7408) is synchronized to the CRTC by using the clock signal (3.072 MHz), enabling the CPU to carry out processing without wait cycles. An access to the memory is only possible at every second cycle (interleaving mode). The internal (CPU) data and address busses are connected to the system busses.

3.1 Address Decoding

The addresses that are decoded are as follows:

- Al5 and Al4 define 16 kByte memory blocks
- A7 and A6 are decoded for chip enable and I/O port
- A0 and A1 are routed:
 - to the CRTC for register select and read/write
 - to the CTC for channel select (0 and 1) and
 - to the USART for C/D (control/data indication)

3.2 Reset

The Reset, which is connected to the CPU via two Schmitt-triggers (item 7479 - 7480 in new layout), is either created by a CR-network as power-on Reset, or comes from the distribution board.

3.3 Interrupt Mode

The CTC, which works in interrupt mode 2, is connected to the interrupt line. In interrupt mode 2, the interrupting peripheral device selects the starting address of the interrupt service routine by placing an 8-bit address vector on the data bus during the interrupt acknowledge cycle.



Detailed Description and Servicing Terminalboard - CPU

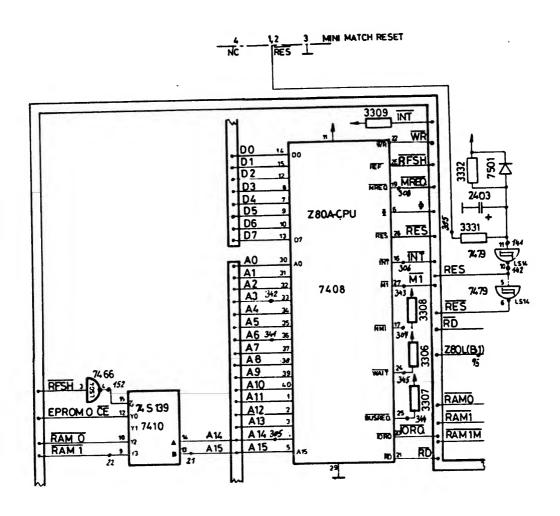


Figure 3.2 Circuit Diagram - CPU

Detailed Description and Servicing Terminalboard - CPU



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Detailed Description and Servicing Terminalboard - CRT Controller

1 GENERAL

The CRT Controller (CRTC) is an MC 6845, which generates all the signals required for controlling a monitor. The video refresh addresses given by the CRTC are only used to control the alphanumeric characters and the attributes. If RAM Bankl is used as a graphic memory the addresses are created by an extra counter, synchronised to the MC 6845.

Full details of the MC 6845 CRT Controller can be found in the relevant data sheets.

The CRTC functional block diagram is shown below:

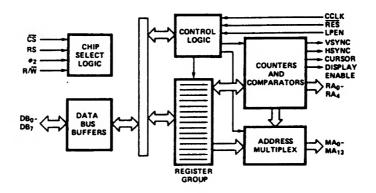


Figure 3.2 CRTC MC 6845 - Block Diagram

Detailed Description and Servicing Terminalboard - CRT Controller



2 BLOCK DIAGRAM

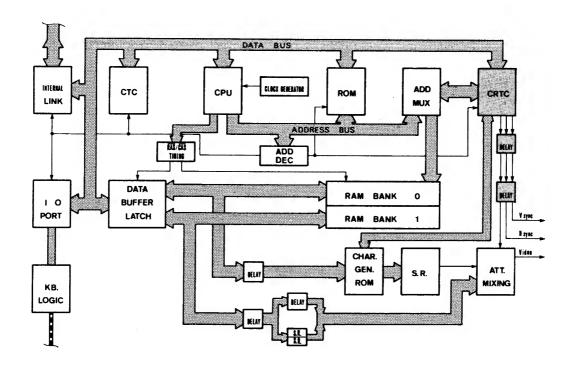


Figure 3.3 P2000C - CRTC Block Diagram



Detailed Description and Servicing Terminalboard - CRT Controller

3 CIRCUIT DESCRIPTION

If the CRTC (item 7412) address lines are routed to the RAM, an 8k Byte video memory is created. The application of +5V (by jumper) to the video memory selects a loop of either 4k Byte (5V on MA11) or 2k Byte (5V on MA12), where hardware scroll is possible. The rest of the video memory is free for the CPU.

The different screen sizes for alphanumeric or graphic displays are programmable.

The video refresh addresses are fed, via a multiplexer, to the RAM's. The read out data is first stored in latches and then fed to the character generator (ROM) as addresses. The lower 4 addresses for the ROM are kept ready as row addresses by the CRTC.

Data from the character generator ROM is read into the shift register and shifted out by the dot clock. After this the attributes, the cursor and the CRTC signal Display Enable (DE) are added. The cursor and the DE signal, together with the Vertical and Horizontal sync signals, are delayed twice (items 7452/7454) to ensure that they are present at the output simultaneously with the data. This delay is not required at the row addresses.

The character clock is used for timing. The light pen input and the light pen register are used to scan the keyboard

3.1 Communication between Z80 and 6845

The inverted IORQ-N signal is used as the system clock for the CRTC. AO and Al of the CPU are used for register selection and R/W selection. It ensures that the R/W signal is present at the same time as the address, i.e., ahead of the rising edge of the system clock. It leads to the following address reservations:

- \$ 80 write address register
- \$ 81 write register
- \$ 82 read status register
- \$ 83 read register

Detailed Description and Servicing Terminalboard - CRT Controller



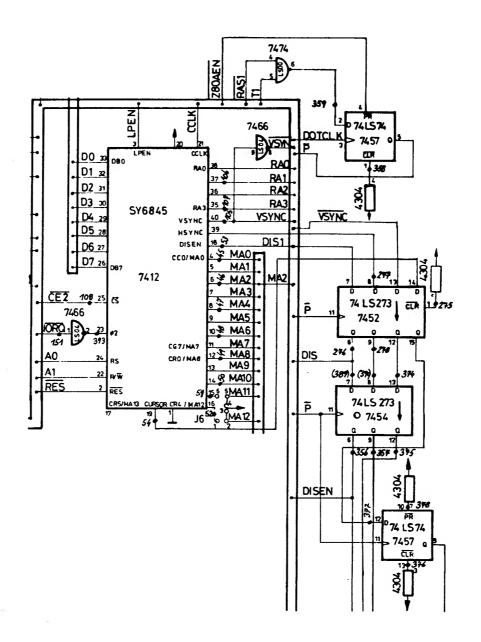


Figure 3.4 Circuit Diagram - CRT Controller





Detailed Description and Servicing Terminalboard - Timing

1 GENERAL

All frequencies on the Terminal board are derived from the dot clock (12.288 MHz), which shifts the dots out of the shift register. This frequency is generated by a quartz crystal controlled Colpitts oscillator.

Detailed Description and Servicing Terminalboard - Timing



2 BLOCK DIAGRAM

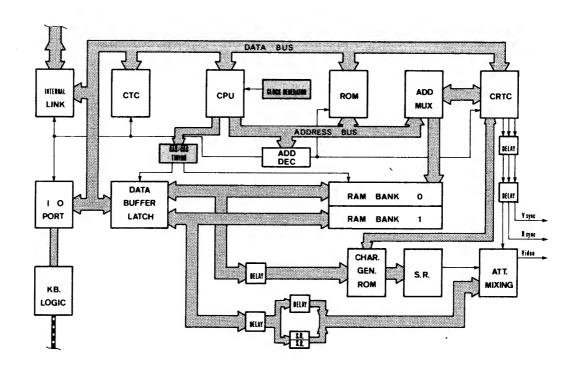


Figure 3.5 P2000C - Timing Block Diagram





Detailed Description and Servicing Terminalboard - Timing

3 CIRCUIT DESCRIPTION

The RAS-N signal, given by 'dot clock/4' via item 7458 - QB13, is applied to the RAM's continuously.

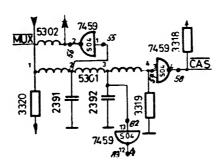
The character clock for the CRTC is derived from 'dot clock/8' via item 7458 - QC/12.

The Z80 address enable (Z80AEN) is produced via a flip flop (item 7463). It is delayed for 162 ns to the character clock. The RAS-N signal releases a read or write signal (alternating the addresses of the CPU or CRTC) in the dynamic memories. This RAS-N signal always appears in the second half of the Z80AEN state, allowing the particular addresses to stabilize.

The MUX-N signal (used to switch over the row addresses to the column addresses), the CPU clock and the CAS-N signal (clock for the CPU and column address strobe for the dynamic memories) are derived from the RAS-N signal by a delay line (item 5301).

3.1 Delay Line

The delay line is a network containing three inductors and two capacitors, as shown in the following diagram:



The delay at the outputs between:

RAS-N and MUX-N is 20 ns RAS-N and CLOCK is 32 ns RAS-N and CAS-N is 50 ns

Detailed Description and Servicing Terminalboard - Timing



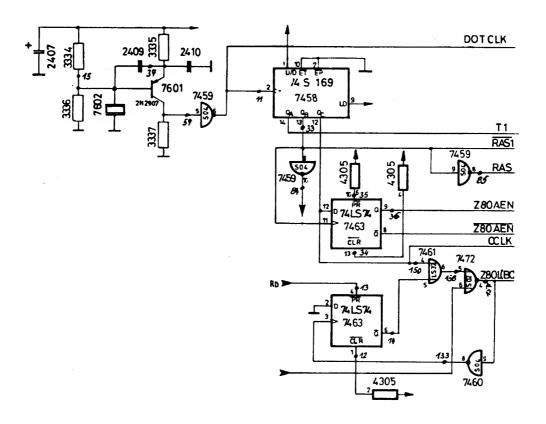


Figure 3.6 Circuit Diagram - Timing





Detailed Description and Servicing Terminalboard - RAM Banks

1 GENERAL

The devices used for the two RAM Banks on the Terminalboard are uPD 416C-5's. Each Bank consists of 8 of these 16K 1-bit RAM's:

- Items 7433 to 7440 are used for RAM BankO, the Video Refresh Memory.
- Items 7425 to 7432 are used for RAM Bankl, the Attribute Memory.

Full details of the uPD 416C-5 can be found in the relevant NEC Data Sheets

Detailed Description and Servicing Terminalboard - RAM Banks



2 BLOCK DIAGRAM

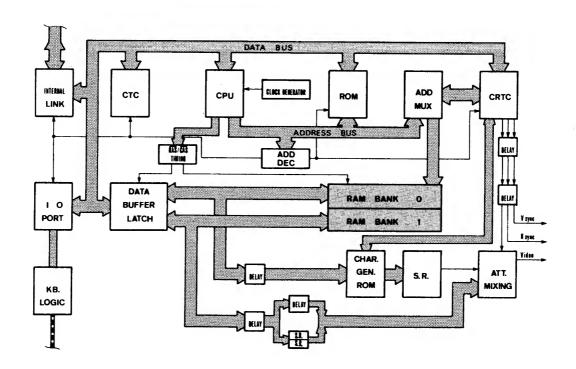


Figure 3.7 P2000C - RAM Banks Block Diagram





Detailed Description and Servicing Terminalboard - RAM Banks

3 CIRCUIT DESCRIPTION

3.1 RAM BankO - Video Refresh Memory

The 16 Kbyte RAM BankO is divided into two parts. The upper part (the higher addresses) contains the video refresh memory for the alphanumeric presentation. The lower part contains the RAM memory of the CPU (buffer, downloaded Initial Program Load, stack etc.,).

The size of the video refresh memory is variable, and may be set to 2, 4 or 8 Kbytes. The selection of the size of the video memory is carried out with jumper J6 (on the Terminalboard). The CPU uses the remaining memory, i.e., 14, 12 or 8 Kbytes.

3.1.1 JUMPER J6

[6] [5]---MA11 [4] |----5V [3] Links on jumper J6 are short circuited as indicated below, to give the sizes of video refresh memory shown:

5-4; 3-2 for Upper 2K 5-6; 3-2 for Upper 4K 5-6; 1-2 for Upper 8K

[1] [2]---MA12

3.2 RAM Bankl - Attribute Memory

The 16 kByte RAM Bankl is used either as the attribute memory or as the graphics memory. When using RAM Bankl as the attribute memory the free area, depending on the selected size of the video refresh memory, can also be used by the CPU. No opcode fetch is allowed.

3.2.1 ATTRIBUTES

Only the lower five bits of each word are used to store attribute information. The significance of each bit is as follows:

- Bit 0 = Underline
- Bit 1 = Blink
- Bit 2 = Inverse representation
- Bit 3 = Brightness 0 (MSB)
- Bit 4 = Brightness 1 (LSB)

Detailed Description and Servicing Terminalboard - RAM Banks



When handling attributes there are three possible modes, selectable via an output port:

- Z80 RD/WR : Normal write/read access to RAM Bank1 by the CPU
- BLOCK MOVE: Using the Z80A CPU LDIR instruction, a block move operation in BankO will automatically move the corresponding attributes to Bankl.
- BLOCK WRITE: First, the attribute (or combination of attributes) must be written to RAM Bankl. It must then be read out (by software) and latched (in item 7447). On all following write actions (of character information) to RAM BankO it is written to the corresponding location in RAM Bankl. If another attribute is read out from RAM Bankl this new attribute is repeated.

	Z80 RD/WR	BLOCK MOVE	BLOCK WRITE
OUT3	0	1	1
OUT4	1	0	1

3.2.2 GRAPHIC MEMORY

- If RAM Bankl is used for graphic memory there are two possibile methods:
- HIGH resolution graphic with 512 x 252 dots
- MEDIUM resolution graphic with 256 x 252 dots and 4 grey shades.

At both resolutions a mixing with alphanumeric characters without attributes is possible.



Detailed Description and Servicing Terminalboard - RAM Banks

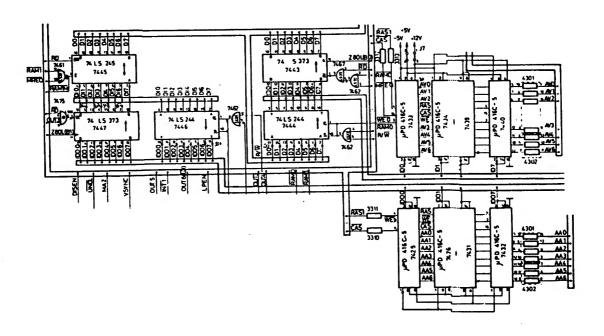


Figure 3.8 Circuit Diagram - RAM Banks

Detailed Description and Servicing Terminalboard - RAM Banks



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2

Detailed Description and Servicing Terminalboard - Address Multiplexer

1 GENERAL

Eight 74 LS 257's are used as the address multiplexer. With this, the addresses of the CPU (AO - Al3) and CRTC (MAO - MAl2) are used alternately to address RAM BankO and RAM Bankl (7-bit addresses).

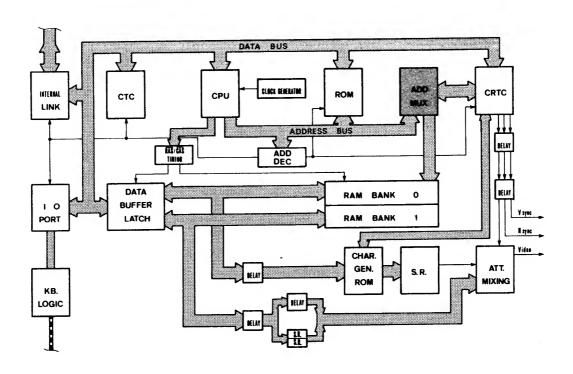


Figure 3.9 P2000C - Address Multiplexer Block Diagram

Detailed Description and Servicing Terminalboard - Address Multiplexer



3 CIRCUIT DESCRIPTION

Two pairs of multiplexers are connected to the address bus of each RAM Bank. The outputs, originating from the CPU and the CRTC, are switched alternately and they are connected with the RAM Address bus. This switch over is done by using the Z8OAEN signal. The MUX-N signal is used to switch over between the lower and higher bits (row address and column address). When the RAS-N signal becomes active (falling edge) the lower addresses are applied to the RAM, so all rows of dynamic RAMs can be refreshed.

At RAM Bankl the addresses of the CRTC are routed via transparent programmable counters to the multiplexer. For alphanumeric representation with attributes the counter is switched so that the supplied addresses appear directly on the outputs (programmable counter 74 LS 197). For graphic mode the counter is switched to count the Z80AEN frequency independent of the data input, if the display is enabled. In this way the whole memory area (16K) of RAM Bankl is read out continuously. The switch over is done by OUTO.





Detailed Description and Servicing Terminalboard - Address Multiplexer

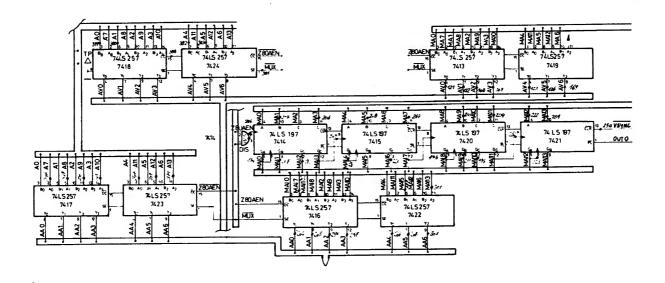


Figure 3.10 Circuit Diagram - Address Multiplexer

Detailed Description and Servicing Terminalboard - Address Multiplexer



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Detailed Description and Servicing Terminalboard - Data Buffer

1 GENERAL

1.1 Temporary Storage

Because of the alternating access to the RAM by CPU and CRTC (162 ns RAS-CPU, 162 ns precharge time, 162 ns RAS-CRTC, 162 ns precharge time) it is necessary to temporarily store data which will be read by the CPU. This does not apply to data which is written to the memory by the CPU, which must only be buffered.

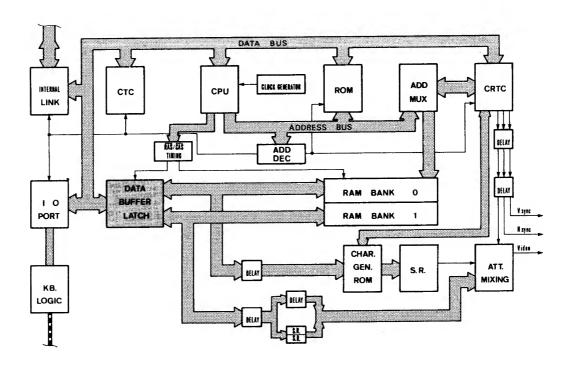


Figure 3.11 P2000C - Data Buffers Block Diagram

Detailed Description and Servicing Terminalboard - Data Buffer



3 CIRCUIT DESCRIPTION

3.1 Read

For reading the data from the memory, a latch signal has to be created. Both RAM Banks are connected to data buffers (BankO 74 LS 244 - item 7444 and Bankl 74 LS 244 - item 7446) and data output latches (RAM BankO 74 S 373 - item 7443 and RAM Bankl 74 LS 373 - item 7447). To switch between different attribute modes (normal, block move and block write), a bus transceiver is added to RAM Bankl (74 LS 245 - item 7445). Every latch (temporary memory) must have a discrete latch signal.

3.1.1 Z80 LATCH SIGNAL FOR RAM BankO (Z80L(B0))

The inverted MUX-N signal, which is only switched at special conditions, is used as the latch signal. This signal always occurs but is suppressed in the event of a read cycle occuring with Tl at the same time as Z80 AEN is high. This is to prevent unstable data being read.

3.1.2 Z80 LATCH SIGNAL FOR RAM Bank1 (Z80L(B1))

The inverted MUX-N signal is used for the latch signal. It is allowed to pass through only if it is the first signal during a RD cycle at which the CCLK and the selected RAM Select Signal are low. In all attribute modes the latch signal can only appear once during the read cycle, otherwise the stored attributes will be destroyed. In modes 2 and 3 the data of the output latch is applied to the input buffer. The Output Control Signal of the output latch will be inverted. The bus transceiver is switched to RAM Bankl only on CPU access.

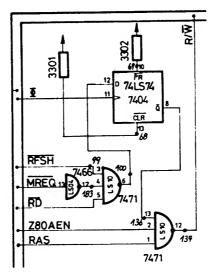


Detailed Description and Servicing Terminalboard - Data Buffer

3.2 Write

In order to write, a R/W-N signal is created. This signal must lead the CPU WR-N signal, otherwise, in some cases, the write cycle cannot be done.

The RAS signal is used to produce the R/W-N signal, requiring both the Z80AEN and the output Q-N of the R/W flip flop (item 7404-2) to be high. This flip-flop controls the RD-N signal with the CPU clock. If the RD-N signals stays at high during the rising edge of the T2 (write cycle) a low is latched and the output Q-N will be high. This allows a R/W-N signal to be produced at the next RAS signal. In order to ensure that the R/W-N signal is only formed during a Memory Write Cycle, the CPU RD-N signal is gated with MREQ-N and RFSH-N to produce a control signal for the flip-flop (item 7404-2).



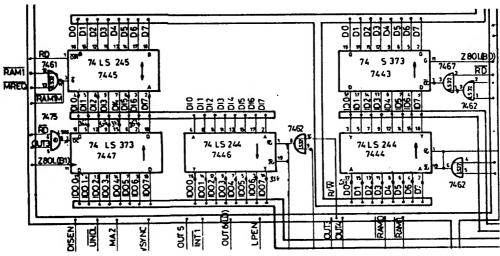


Figure 3.12 Circuit Diagram - Data Buffer

Detailed Description and Servicing Terminalboard - Data Buffer



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Detailed Description and Servicing Terminalboard - Shift Register

1 GENERAL

The purpose of the shift register is to produce serial dot information from the bytes supplied by the character generator ROM and to ensure that all of the signals necessary for video are present at the same time.

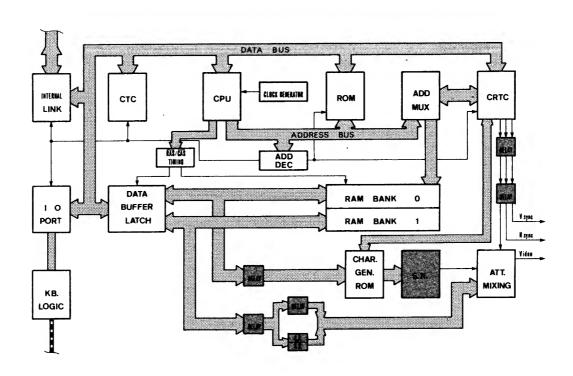


Figure 3.13 P2000C - Shift Register Block Diagram

Detailed Description and Servicing Terminalboard - Shift Register



3 CIRCUIT DESCRIPTION

3.1 Alphanumeric Mode

In alphanumeric mode, the data is read out of the RAM BankO and is stored in a latch (item 7451) at the rising flank of the Z80AEN signal. It is then routed to the character generator ROM (item 7450) as addresses. The row address signals are also applied to the CRTC and the dot information is read out of the character generator ROM. The parallel load (P-N) signal (derived from item 7457) enables the loading of the shift register (item 7449), followed by shifting out of video data.

Attribute information from RAM Bankl is delayed by item 7451 and data from RAM BankO is delayed by item 7453. As the character generator ROM causes a further delay to the data, the attribute information is also delayed once again using a temporary memory (item 7454). This ensures that dot and attribute information are synchronized.

3.2 Graphics Modes

In the high resolution graphics mode the output of the first shift register (item 7456) is connected to the input of the second shift register (item 7455), the output of which is connected to the output buffer (items 7469/7470). So all 8 bits are shifted out in series.

In the medium resolution mode, both outputs of the shift registers are fed in parallel to the output buffer and so define the brightness of the dot. The half dot frequency is used for the shift frequency in this mode. This is why the dots are double sized compared with the high resolution mode.

3.3 Mode Switching

The signals OUTO and OUT1 are used to switch modes.

OUTO switches over between pure alphanumeric and alphanumeric mixed with graphic representation



Detailed Description and Servicing Terminalboard - Shift Register

The 74 LS 399 (data multiplexer with memory - item 7476) switches over between the different modes controlled by OUTO. The memory is neccessary to equalise the different run times of the gates used for attribute mixing. After buffering (by open collector drivers), the Brightness signals and the Display Enable signal are mixed to become the video signal, which is routed to the monitor.

When mixing alphanumerics and graphics, HRO-N with DOT inactive is the same as inverting HRO-N. If DOT is active, the gate (item 7475), ensures that text superimposed on a graphics display is inverted (pixel by pixel). The LS 157 (item 7477) gives improved contrast in high resolution graphics mode.

3.4 Beeper

The beeper (item 7603) is enabled by the signal OUT2 and driven with the UNDL signal. The signal UNDL is the decoded 10th row of a character line, where the underline is set. (1300 Hz).

3.5 Attribute Mixing

ATO = Underline: 10th line is decoded out of ROW information

from CRTC, UNDL-N, and gated with DOT (active

1ow).

AT1 = Blink: VERT SYNC divided by 16 is gated with DOT-N.

(Active high) (This equals 3 changes every 2 seconds). DOT-N

is suppressed each $320 \mathrm{ms}$ to produce BLINK.

NB See Note below.

AT2 = Invert: DOT-N is inverted if AT2 is active.

(Active high)

AT3 = Bright0: These two signals are used to define one of the

AT4 = Brightl: four brightness levels via the 74 LS 399 (item 7476). The C output defines DOT Yes/No

and the A and B outputs define the level.

Note: In the new layout, BLINK is software driven, with OUT 7.

8-4

Detailed Description and Servicing Terminalboard - Shift Register



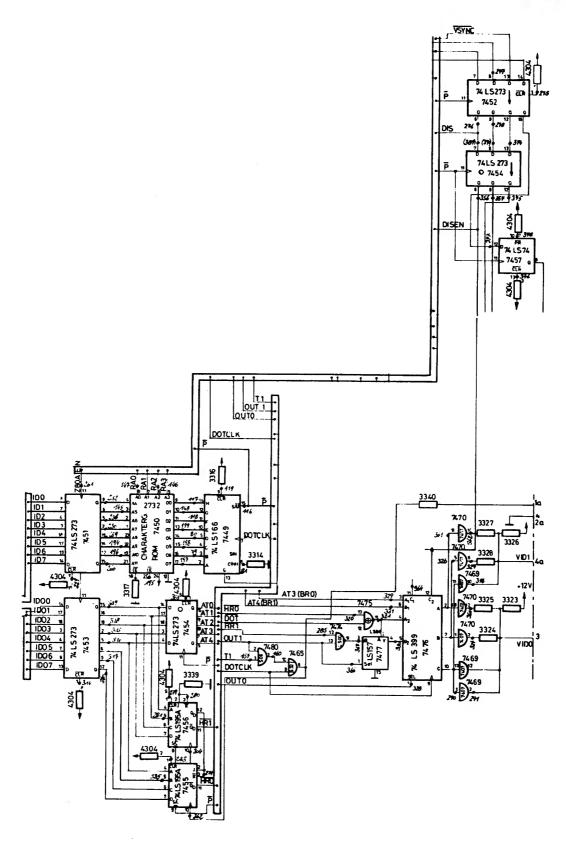


Figure 3.14 Circuit Diagram - Shift Register



Detailed Description and Servicing Terminalboard - Attribute Mixing

1 GENERAL

The purpose of the attribute mixing circuitry is to ensure that, as each character is read out of the character generator, the dot information is modified according to the required attributes.

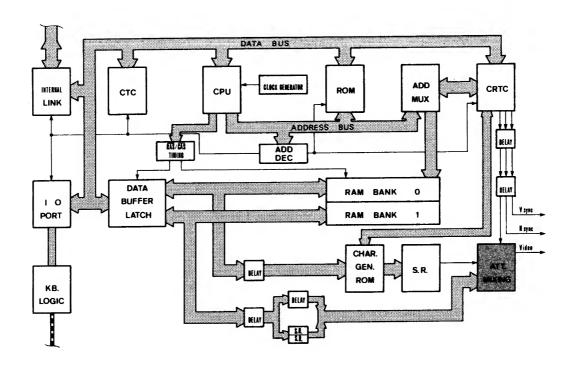


Figure 3.15 P2000C - Attribute Mixing Block Diagram

Detailed Description and Servicing Terminalboard - Attribute Mixing



3 CIRCUIT DESCRIPTION

The signals ATO - AT4, derived from the attribute information in Ram Bankl have the following meanings:

ATO = Underline AT1 = Blink AT2 = Invert

AT3 = Brightness 0 AT4 = Brightness 1

These signals remain valid for the definition of the complete character, i.e., for the full Row Address sequence.

AT3 and AT4 define the brightness level (1-4) as either quarter bright, half bright, normal or bold; and are used to determine the 'bright-up' potential applied to the monitor with each ROW of the character being displayed.

The three attributes defined by ATO - AT2 are carried out by inversion or suppression of the dot information.

- Underline: the dot information for the 10th line of the character is set active

- Blink: the dot information for the complete character is suppressed at a defined frequency

- Invert: the dot information for the complete character is

inverted

10 of item 7474).

9-3



Detailed Description and Servicing Terminalboard - Attribute Mixing

3.1 Underline

ATO is gated with UNDL-N (from row addresses RAO, RA3 and RA1 inverted) and then gated with DOT to set the dot information for the 10th line of a character. This function is carried out with 74 S 00/1-2 (item 7473), 74 LS 10/3 (item 7471), 74 LS 32/2 (item 7467).

3.2 Blink

AT1 is gated with the blink frequency generator signal (derived from VSYNC) to produce a suppression signal at the rate of 3 changes every 2 seconds. During the active period of this signal no character information appears on the screen. This function is carried out with 74 S 00/3 (item 7473), 74 LS 00/3 (item 7474), 74 LS 293 (item 7468).

Note: From Serial No. 3700, BLINK is carried out by software via OUT7 (Item 7468 is removed and OUT7 connected to pin

3.3 Invert

AT2 will produce a complete inversion of the dot information for the character. This function is carried out with 74 LS 86/3 (item 7475), 74 S 08/3 (item 7480).

3.4 Beep

UNDL-N is gated with OUT2 to produce the beep signal.

Detailed Description and Servicing Terminalboard - Attribute Mixing



3.5 Video Signals

For each DOT applied to the 74 LS 399 (item 7476), the level of the video outputs VIDO/VID1 is determined by the setting of AT3/AT4 and the resultant A & B outputs. Via the open collector gates (items 7469/7470), one of four levels of video signal will be produced.

In the event of NO DOT being applied, the C output will be active, driving the video outputs to ground (low) potential. Due to the characteristics of the internal monitor, the aiming potential for the video signal, VIDO, is +12V and an additional gate has been incorporated to handle the higher current. This is not required for the external monitor, where the aiming potential for VID1 is +5V.

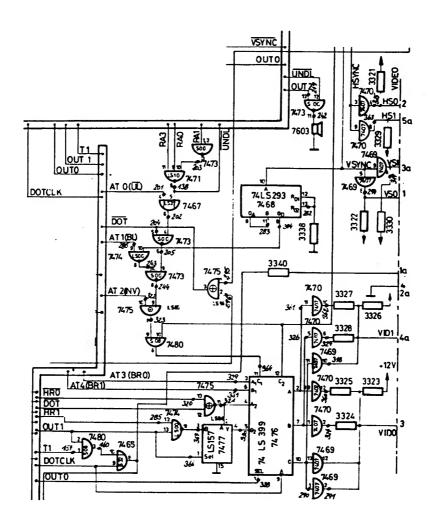


Figure 3.16 Circuit Diagram - Attribute Mixing



1

Detailed Description and Servicing Terminalboard - Character Generator ROM

GENERAL

The character generator ROM is a $4K \times 8$ bit device - 2632, (item 7450) giving 256 characters in a 16×8 matrix. Only the first 12×8 bits are used to define a character, the contents of the remaining 4×8 bits being undefined and not addressed by the CRTC. See Appendix A for the Character Generator listing.

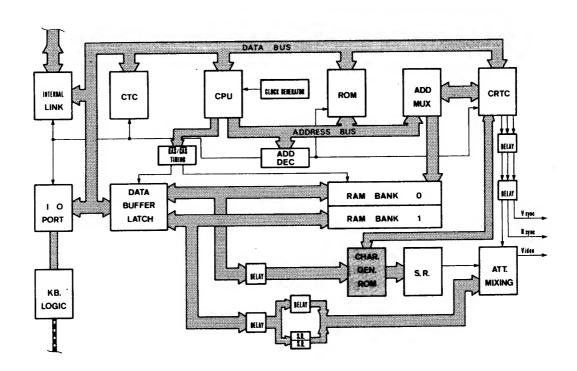


Figure 3.17 P2000C - Character Generator ROM Block Diagram

Detailed Description and Servicing Terminalboard - Character Generator ROM



3 ADDRESSING

A character is read out of the ROM by clocking out, byte by byte, the 12 bytes that are used to represent that character.

Address lines IDO - ID7 are first latched from Ram BankO. (A4 - A11 on the character generator = 000x - 0FFx). This identifies the start address in ROM of the required character.

The Row Address lines RAO - RA3 are then activated in sequence by the CRTC (AO - A3 on the character generator = 0 - F, but programmed within the CRTC to count to 12; i.e., 0 - B). One byte of ROM is clocked out to the shift register (item 7449) with each increment of the character clock.

Subsequently the information is shifted out of the shift register, bit by bit, with the least significant bit first.

3.1 Character Representation in ROM

As an example of the ROM contents, the following is the information that represents the letter 'B':

FF C1 BD BD C1 BD BD C1 FF FF FF

where 0 (\bullet in illustration below) = bright in normal character display and 1 (\cdot in illustration) = dark.

$\mathbf{F}\mathbf{F}$	=	•	•	•	•	•	•	•	•
C1	=	•	•	•	•	•	•	•	•
BD	=	•	•	•	•	•	•	lacktriangle	•
BD	=	•	•	•	•	•	•	lacktriangle	•
C1	=	•	•	•	•	•	•	lacktriangle	•
BD	=	•	•	•	•	•	•	•	•
BD	=	•	•	•	•	•	•	lacktriangle	•
C1	=	•	•	lacktriangle	lacktriangle	lacktriangle	lacktriangle	lacktriangle	•
$\mathbf{F}\mathbf{F}$	=	•	•	•	•	•	•	•	•
$\mathbf{F}\mathbf{F}$	=	•	•	•	•	•	•	•	•
FF	=	•	•	•	•	•	•	•	•
שש	_	_		_		_	_	_	_

Figure 3.18 Character Representation in ROM





Detailed Description and Servicing Terminalboard - CTC

1 GENERAL

The Terminalboard uses the same Z80A CTC device as used on the Mainboard (Z8430A). Further information is given under the section describing the Mainboard CTC's.

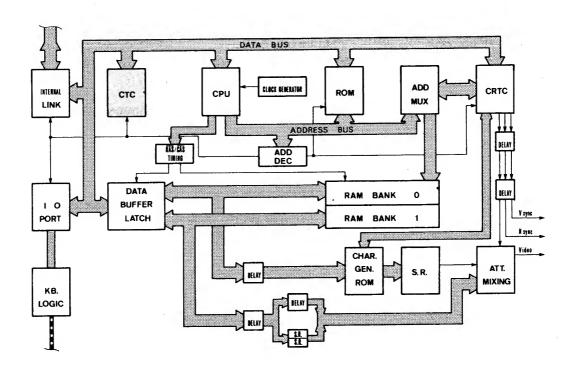


Figure 3.19 P2000C - CTC Block Diagram

Detailed Description and Servicing Terminalboard - CTC



CIRCUIT DESCRIPTION

The Z80 CTC contains 4 programmable counters and carries out all interrupts in mode 2.

Channel 0 : I/O address 00 - Baud-rate generator

Input frequency of this channel is the system clock signal divided by 5 and output of this channel is the clock for the USART:

CLK

3,072 MHz

CLK/5 TO₀/2 614,400 kHz

for USART (duty cycle 50%)

Channel 1: I/O address 01

Input of this channel is the USART transmitter ready signal and starts USART transmitter interrupts.

Channel 2: I/O address 02

Input of this channel is the USART receiver ready signal and starts USART receiver interrupts.

Channel 3: I/O address 03

The input of this channel is connected to the INT1-N of the keyboard logic and starts the interrupt for the keyboard handling.





Detailed Description and Servicing Terminalboard - CTC

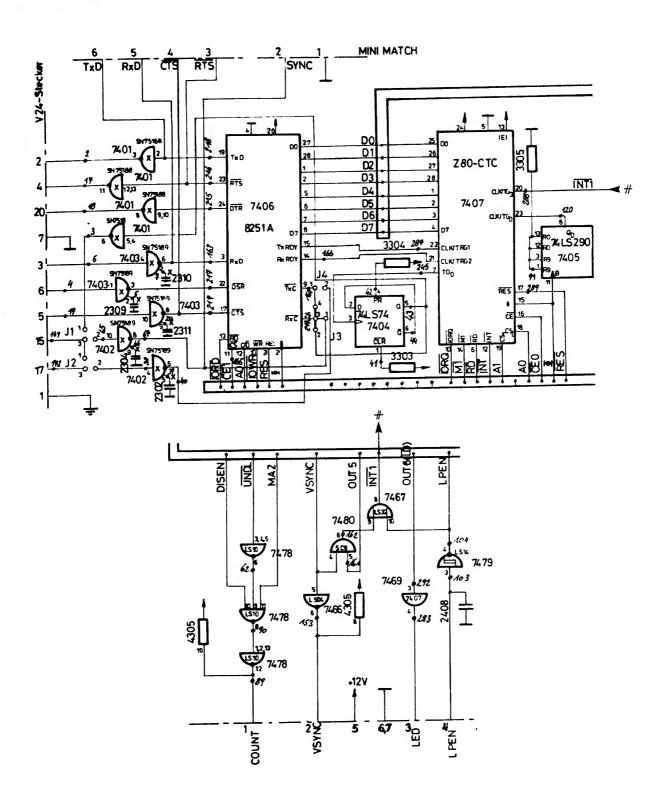


Figure 3.20 Circuit Diagram - CTC

Detailed Description and Servicing Terminalboard - CTC



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Detailed Description and Servicing Terminalboard - V24/Internal Interface

1 GENERAL

The optional V24 connection and the internal link to the Mainboard is controlled by a USART 8251A (item 7406) identical to that used on the Mainboard. Further information on the device can be found in that section.

The link connection to the Mainboard is direct, at TTL levels; the V24 connections (used only when the Terminalboard is used as a stand-alone terminal) are buffered by open collector devices (items 7401, 7402 and 7403).

The receiver and transmitter clocks may be internal (CTC channel 0) or external; selected by Jumpers J1 to J4.

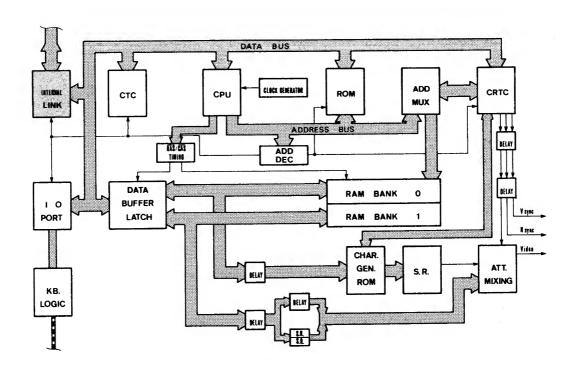


Figure 3.21 P2000C - V24/Internal Interface Block Diagram

Detailed Description and Servicing Terminalboard - V24/Internal Interface



3 CONNECTIONS

3.1 Internal Link Connector

The connections are reversed in comparison to the internal link connector on the Mainboard. The pinning is as follows:

Tb	Pin	Signal	Mb	Pin
	1	GND		6
	2	SYNC		5
	3	RTS-N		4
	4	CTS-N		3
	5	RxD		2
	6	TxD		1

3.2 V24 (Optional) Connector

The optional V24 connector includes the standard V24 connections and two pins for external sync signals in conjunction with jumpers J1 to J4. The pinning is as follows:

Pin	Signal
1	Protective GND
2	TxD
3	RxD
4	RTS-N
5	CTS-N
6	DSR-N
7	GND
15	Ext Rx Clock
17	Ext Tx Clock
20	DTR-N

3.3 Jumpers

In the standard configuration, the V24/Internal interface operates with the jumpers J1 - J4 set as follows:

J1 - No links

J2 - No links

J3 - Links between 4 and 3

3 and 2

3 and 1

J4 - No links



Detailed Description and Servicing Terminalboard - V24/Internal Interface

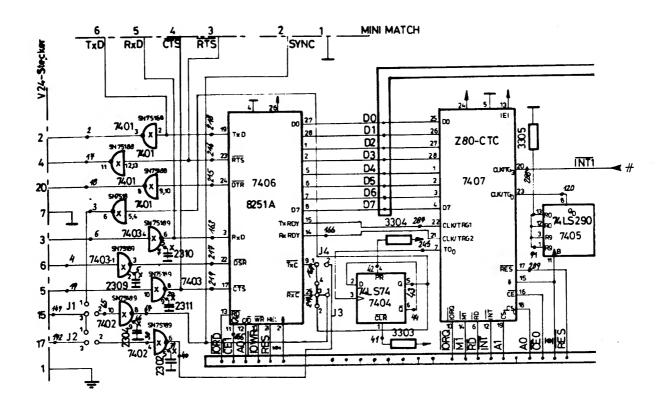


Figure 3.22 Circuit Diagram V24/Internal Interface

Detailed Description and Servicing Terminalboard - V24/Internal Interface



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Detailed Description and Servicing Terminalboard - Address Decoder

1 GENERAL

As mentioned in the CPU description, some of the CPU addresses are decoded as detailed in the following paragraphs.

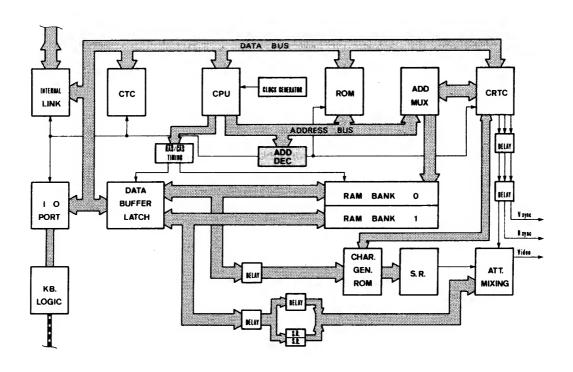


Figure 3.23 P2000C Address Decoder - Block Diagram

Detailed Description and Servicing Terminalboard - Address Decoder



3 CIRCUIT DESCRIPTION

3.1 Address Lines A14 - A15

A14 and A15 are decoded by a 74 S 139 (item 7410), controlled by RFSH-N from the CPU, to produce RAMO-N and RAM1-N for the selection of RAM Banks O and 1. These addresses are also used to produce the EPROM O CE-N signal which is used as the CS-N input for the Program ROM (item 7409).

3.2 Address Lines A6 - A7

A6 and A7 are decoded by the other part of item 7410, controlled by the signal M1-N from the CPU, to produce chip enable signals for the CTC (CEO-N), the USART (CE1-N) and the CRTC (CE2-N). These addresses are also used to produce the signals OUT-N and IN-N, (by gating with I/O, read and write signals) for controlling data I/O (items 7441/7442).

3.3 Address Lines A0 - A1

AO and Al are linked directly to the CNTR bus, where they are

- at the USART for control/data indication (C/D-N with AO)
- at the CTC for chip select (CSO:AO CS1:A1)
- at the CRTC for read/write indication (R/W-N with A1) and register select (RS with A0)



Detailed Description and Servicing Terminalboard - Address Decoder

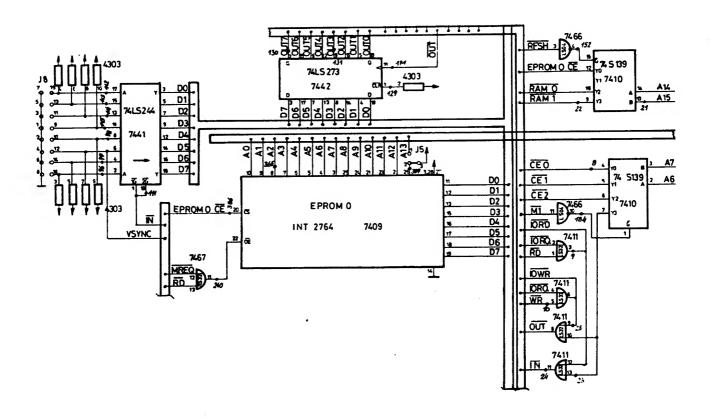


Figure 3.24 Circuit Diagram - Address Decoder

Detailed Description and Servicing Terminalboard - Address Decoder



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Detailed Description and Servicing Terminalboard - Keyboard Logic

1 GENERAL

To reduce the number of connection lines between the Keyboard and the Terminalboard a serial interface is used. To make this possible the system uses a counter (fitted inside the keyboard) which is controlled by the video refresh address MA2.

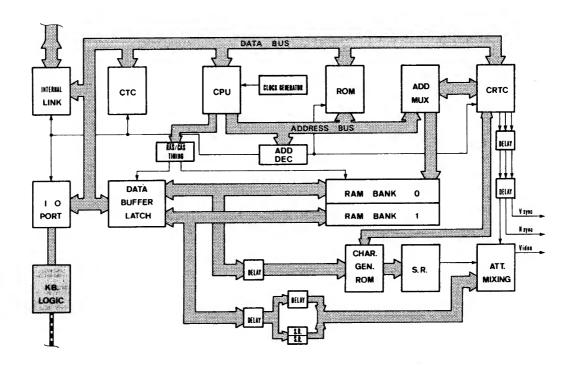


Figure 3.25 P2000C Keyboard Logic - Block Diagram

Detailed Description and Servicing Terminalboard - Keyboard Logic



3 CIRCUIT DESCRIPTION

MA2 is used as a clock, and is gated by UNDL-N on the 10th row of each character line. The counter 'counts up' to 10 in each character line, controlling the inputs to a 16 to 1 data selector, the first 10 inputs of which are the columns of the keyboard (10 column x 16 row) key matrix. The overflow of the decimal counter is used to control a binary counter, which applies a low signal to each of the 16 rows of the key matrix in turn.

On the keyboard key matrix, rows 1 to 10 are used for normal keys and rows 12 - 15 are used for special functions (control, shift, shift lock, supershift).

When the active row and column co-incide with a pressed key, the output of the data selector goes high, sets a flip-flop, and releases a light pen strobe. As the light pen strobe co-incides with a video refresh address (which distinguishes the pressed key), this address is loaded to the light pen register by the CRTC.

A further key depression in the same scan period will cause the new key, which may be a special function key from rows 12-15, to be encoded. Only one special function key is allocated to each of these four rows. In order to allow enough time for interrupt handling the 11th row is not used. The 16th row is used to disable the counter input.

The VSYNC signal is used to reset the counters. The LED in the shift lock key can be set with OUT6. An interrupt is released by the light pen strobe via CTC. The interrupt routine sets OUT5 and enables an interrupt by VSYNC. When an interrupt (by VSYNC) appears it will wait for the light pen strobe. A repeat function is built in when a key remains depressed, giving a sufficient pause for normal keyboard handling not to cause unwanted repeats.

Because the CRTC is programmed for 24 rows per page but the key board matrix consists of 16 rows only, the counter input is locked from row 16 and is opened again with the next VSYNC.





Detailed Description and Servicing Terminalboard - Keyboard Logic

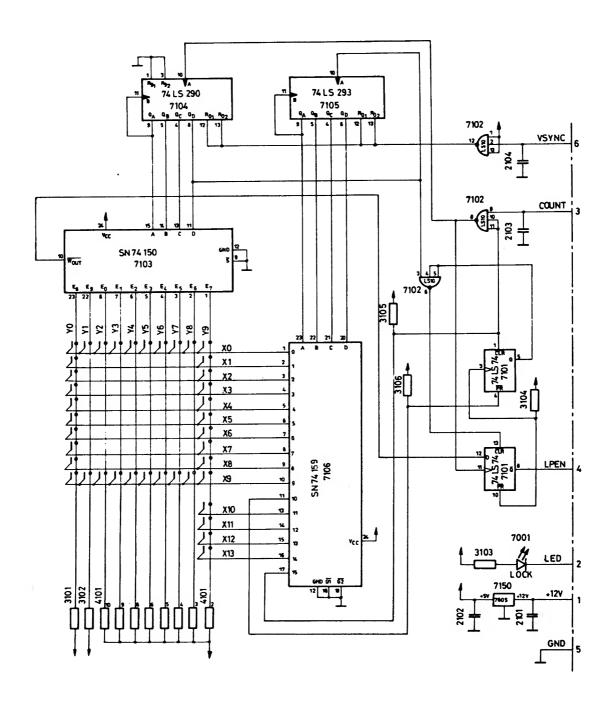


Figure 3.26 Circuit Diagram - Keyboard Logic

Detailed Description and Servicing Terminalboard - Keyboard Logic



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Detailed Description and Servicing Terminalboard - I/O Ports

1 GENERAL

The Terminalboard I/O ports are given in the table in paragraph 3.

2 BLOCK DIAGRAM

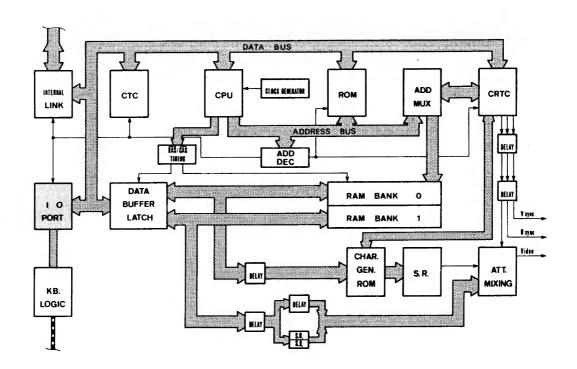


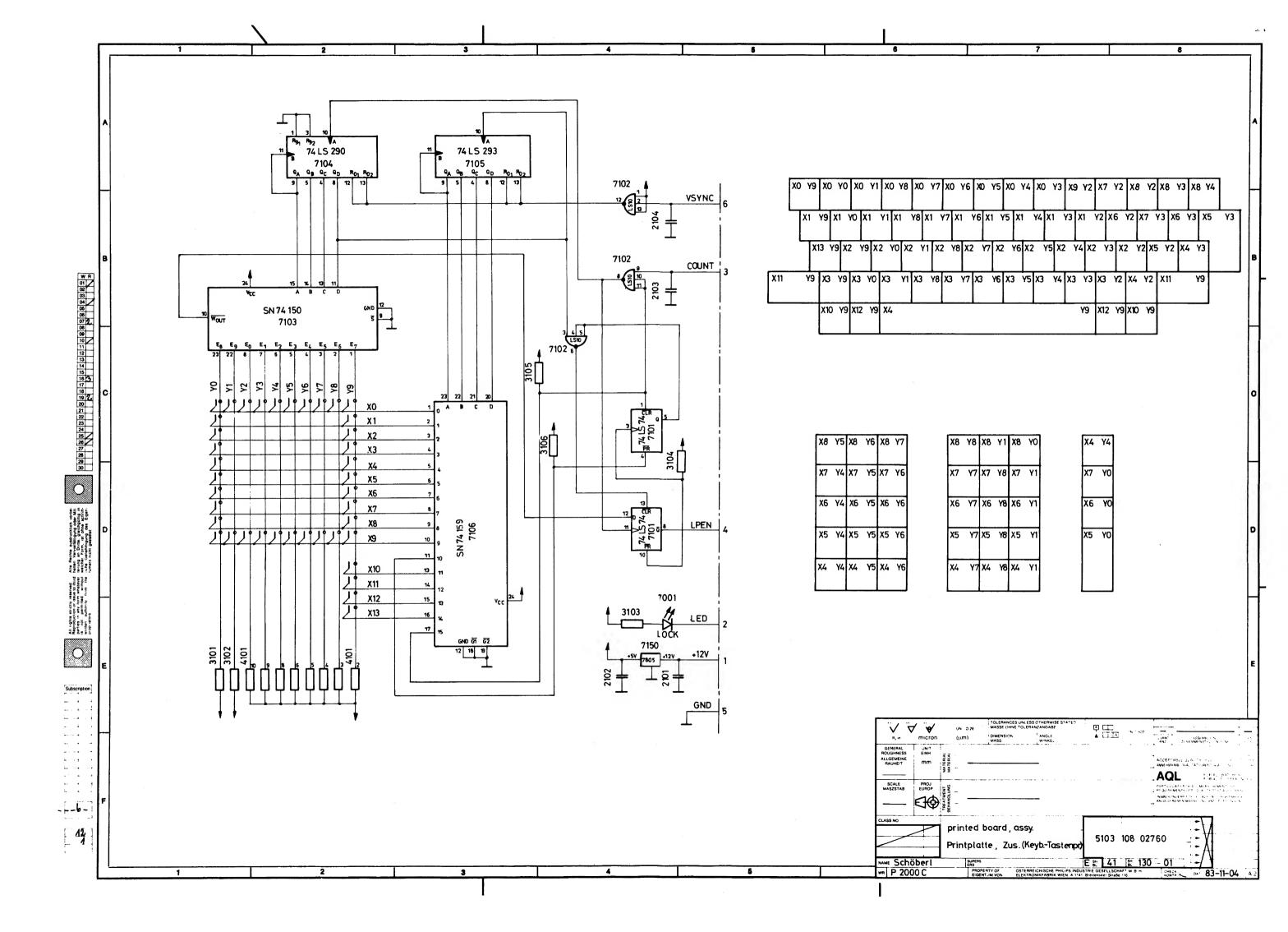
Figure 3.27 P2000C I/O Ports - Block Diagram

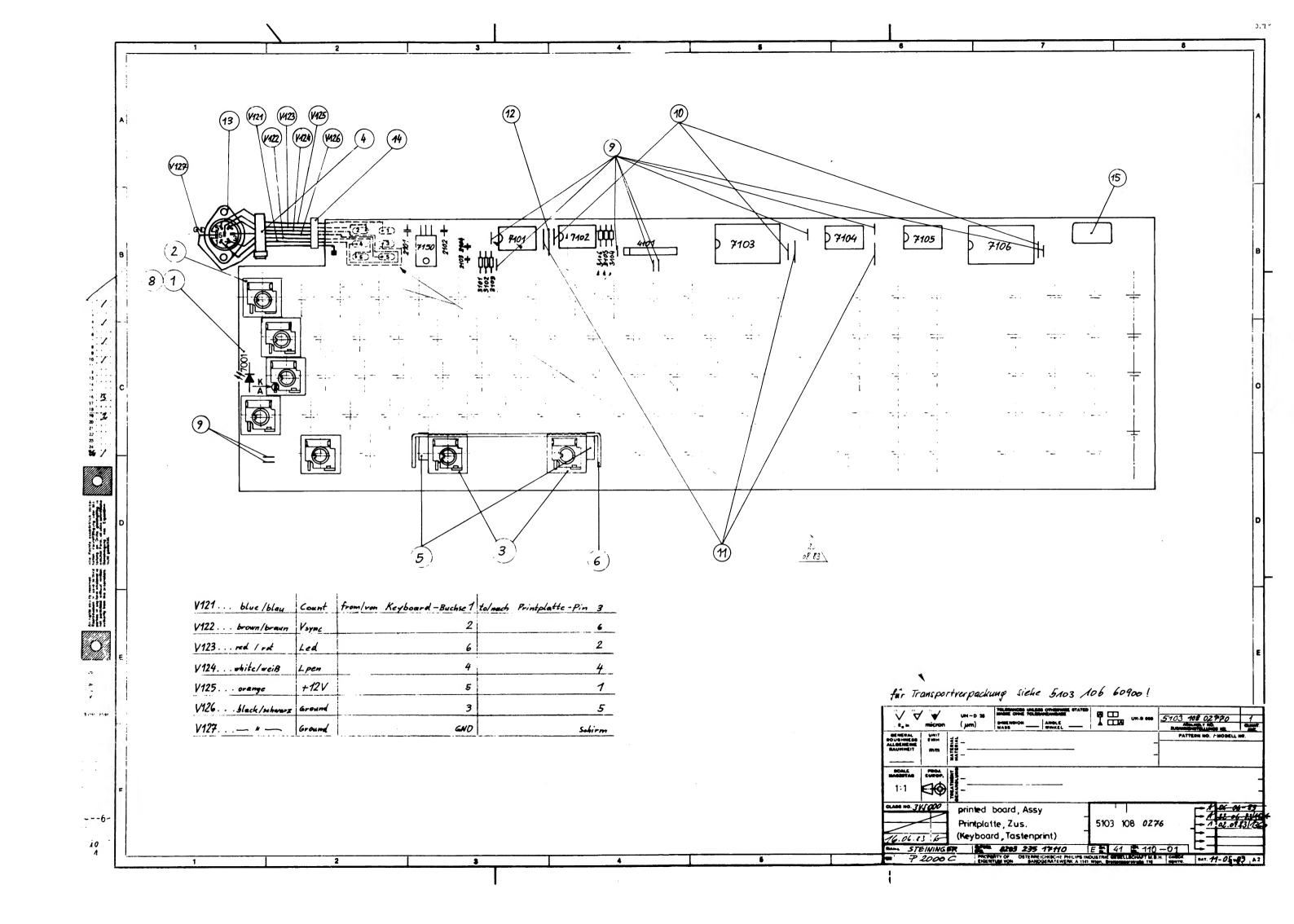
Detailed Description and Servicing Terminalboard - I/O Ports



3 I/O PORTS

Port	Use
00 - 3F	CTC read & write
40 - 7F	8251 USART read & write
80 - BF	CRTC 6845
80	write address register
81	write register
82	read status register
83	read register
CO - FF	IO Ports (OUTO - OUT7, INO - IN7)
OUTO	alphanumeric/graphic mode
OUT1	high resolution/half resolution
OUT2	beeper
OUT3	block move/block write
OUT4	block move/block write
OUT5	vertical sync interrupt enable
ou t 6	shift lock LED
OUT7	blink
IN5	vertical sync input









Detailed Description and Servicing Keyboard

1 GENERAL

The keyboard has been specially designed for the P2000C microcomputer, with particular attention having being paid to the ergonomic requirements of the professional user. It is a low profile unit with sculptured keys on the typewriter section and has separate function and numeric pads. An LED is incorporated in the 'shift lock' key to indicate that the keyboard is in the shift lock mode.

The keyboard is separate from the main unit and connected by a spiral cable. It contains only the keyswitch matrix and a few TTL packages, which reduces the number of wires required in the connecting cable.

For transportation the keyboard fits inside the facia of the main unit and is secured by the carrying strap. The keyboard connecting cable is stowed, with the mains cable, in a compartment at the back of the unit.

1.1 National Versions

Although the keyboard is obtainable in various National Versions, the electronics of each is identical and only the keytops differ. The adaptation of the basic keyboard to meet national requirements is carried out by the use of the Keyboard and Video Tables. (See CP/M Configuration Program).

This chapter contains illustrations of two of the National keyboards - Austrian/German and United Kingdom.

Detailed Description and Servicing Keyboard



2 CIRCUIT DESCRIPTION

The keyboard is scanned in synchronization with video refresh operation of the CRTC. At each key depression the light pen input is activated and the key is identified by means of the light pen register in the CRTC. (This restricts the use of the keyboard to functioning with the video circuits).

Key rollover and key lockout depends on the position of the key in the scanning row. If the 'key 2' is depressed while 'key 1' remains depressed; two situations are possible:

- If 'key 2' stands later in the scanning row than 'key 1',it will be encoded when 'key 1' has been released.
- If 'key 2' stands earlier in the scanning row it will be encoded immediately.

Special keys (shift, supershift, control and shift lock are encoded whenever they are depressed.

The circuit action is described further under Terminalboard - Keyboard Logic.

2.1 Pinning

The keyboard cable 5103 107 81270 with 2 plugs 6-pole DIN 45 322 (240°) has the following pin designation:

PIN	SIGNAL	I/O
1	count	0
2	vertical sync	0
3	1ed	0
4	light pen	I
5	+12v	0
6	gnd	0
screeni	ng to gnd	





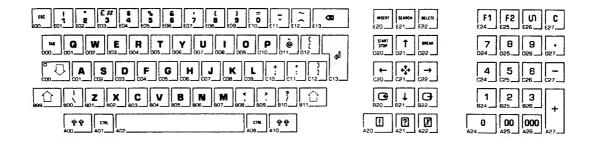
Detailed Description and Servicing Keyboard

3 NATIONAL VERSION KEYBOARDS

3.1 National Version Keyboard - Austrian/German

ESC 1 2 3 4 5 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6	7 () = ? 7 8 9 0 E10 E11 B E12 E13	FUGEN SUCHEN LOSCH E20 E21 E22	F1 F2 M C
Q W E R T 2	2 U I O P Ü + O P Ü +	START AB-	7 8 9 , 024 025 026 027
COO COS COS COS COS COS COS COS COS COS	H J K L Ö Ä 🗍	← C20 C21 C22	4 5 6 - C24 C25 C26 C27
899 800 801 802 803 804 805.	N N ; : - 10 811	B20 B21 B22	1 2 3
400 CTRL ADS	CTML	A20 A21 A22	0 00 000 A27_

3.2 National Version Keyboard - United Kingdom



Detailed Description and Servicing Keyboard



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Detailed Description and Servicing
Monitor

1 GENERAL

The P2000C incorporates a Mitsubishi Electronic Corporation Model NT-1002XU, 9" Monochrome (Green) Monitor. The maintenance philosophy for this unit is that it should be 'serviced by replacement' and, consequently, full technical details will not be supplied. However, this section outlines the safety precautions to be taken when handling and using the unit and will give instructions on any adjustments that may needed.

2 SAFETY PRECAUTIONS

HIGH VOLTAGE WARNING

Parts of the CRT PCB are supplied with HIGH VOLTAGE (700V), and extreme care must be taken in handling the unit when it is switched 'ON'.

Even after switching 'OFF', the CRT ANODE may be at a dangerous voltage level. This high voltage should be discharged to ground after the ANODE CAP has been carefully removed.

HIGH VOLTAGE WARNING

In addition to precautions against fatal electric shock, the following points should be considered when handling or using the Monitor:

- Although an anti-explosive type CRT is used in the Monitor, any damage to the tube is potentially dangerous. Care must be taken in handling the Monitor to ensure that the surface of the CRT is not damaged. Remember that any damage to the tube will affect both SAFETY and PICTURE QUALITY.
- The anode cap is held firmly in place by the cap spring. Ensure that this item is always fitted.
- To preserve 'tube life', it is advisable to use the lowest acceptable brightness level for the display. This will lessen the effect of phosphor burn on the tube.

Detailed Description and Servicing Monitor



- Avoid moving the sub-magnets on the deflection yoke, which compensate for linearity and raster distortion. Extreme care should be taken when handling the deflection yoke to avoid damage to the wiring.

3 ADJUSTMENTS

HIGH VOLTAGE WARNING

Adjustments to the Monitor must only be carried out by a qualified Service Technician.

HIGH VOLTAGE WARNING

Connect appropriate power source and TTL signals to the module as follows:

Power Source DC 12V +/-0.2V Video TTL positive 5V P-P Vertical Sync TTL negative 5V P-P Horizontal Sync TTL positive 5V P-P

The following procedures outline adjustments for individual stages:

3.1 Horizontal Frequency (VR501)

- Disconnect input signal
- Connect a frequency counter (loose coupling) to horizontal output
- Adjust VR501 for output of 15.67 KHz

3.2 Vertical Frequency (VR401)

- Connect input signal
- Adjust VR401 to stabilize picture in vertical plane



Detailed Description and Servicing
Monitor

3.3 Horizontal Width (L502)

- Input full dots test pattern at appropriate brightness level
- Adjust L502 to give horizontal width of 165 +/- 2mm

3.4 Vertical Height (VR402) and Vertical Linearity (VR403)

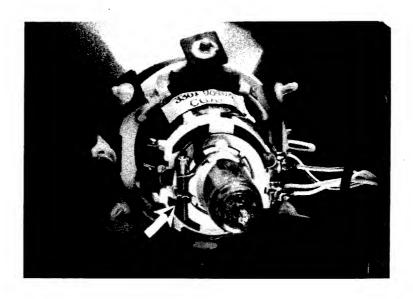
- Input cross-hatch test pattern
- Adjust VR402 and VR403 to obtain required vertical height with best possible vertical linearity

3.5 Picture Centering

- Rotate the two 'centering magnetic rings' of the deflection yoke to centralize the display on the CRT screen.

If the displayed data is 'tilted', this may be corrected by loosening the screw holding the deflection yoke and rotating the yoke to correct the display.

Note: The deflection yoke must be pushed home firmly before tightening the screw.



3.6 Focus (VR203)

- Adjust VR203 to obtain best possible focussing within the display area.

Detailed Description and Servicing Monitor



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Detailed Description and Servicing Disk Drives

1 GENERAL

The Flexible Disk Drives fitted to the P2000C are the TEAC Corp 5½" Slim Line FD-55 drives. Two versions are available:

TEAC FD 55A - 160K Single Sided, single track density (48tpi) TEAC FD 55F - 640K Double Sided, double track density (96tpi)

Information available at publication date indicates that these drives will be superceded by the "L" version of each type:

TEAC FD 55A (L) and TEAC FD 55F (L)

Information concerning the operation and servicing of these drives is available from the manufacturer, and interested readers are referred to the following specifications:

TEAC FD 55A Spec P/N 10530146 - 00A TEAC FD 55F Spec P/N 10530146 - 03A

TEAC FD 55A(L) Spec P/N 10530160 - 00A TEAC FD 55F(L) Spec P/N 10530160 - 03A

Detailed Description and Servicing Disk Drives



2 OPERATIONAL CHARACTERISTICS

The following characteristics are extracted from the specifications for the various drives mentioned in paragraph 1.

2.1 Data Capacity

Data capacity assuming MFM recording:

	640 K	160K
Data transfer rate (K bits/sec)	250	250
Tracks per disk	160	40
Inner track bit density (bpi)	5,922	5,536
Inner track flux density (frpi)	5,922	5,536
K bytes/track - Unformatted	6.25	6.25
K bytes/disk - Unformatted	1000	250
K bytes/sector - Formatted	0.256	0.256
K bytes/track - Formatted	4.096	4.096
K bytes/disk - Formatted	655.3	163.84
(formatted = 16 sectors per track)		

2.2 Disk Rotation Mechanism

All types.

- Spindle motor:	Direct DC brushless
- Spindle motor speed:	300 rpm
- Motor servo:	Frequency servo by AC
	tachometer
- Motor/spindle connection:	Motor shaft direct
- Disk speed:	300 rpm
Long term speed variation (LSV):	Less than $+/-1.5\%$
Instant speed variation (ISV):	Less than +/- 1.5%
- Start time:	Less than 400msec
- Average latency:	100msec





Detailed Description and Servicing Disk Drives

2.3 Index

All types.

- Number of index:

- Detection method:

- Detection cycle:

- Index/alignment dipole spacing:

1 per disk revolution LED and photo-transistor

200 msec + /- 1.5%

0 - 400usec, with specified test disk

2.4 Track Construction

	640 K	160K
Track density:	96tpi	48tpi
Number of cylinders:	80	40
Number of tracks per surface:	80	40
Number of tracks per disk:	160	40
Outermost track radius (track 00)	Side 0 57.150mm	57.150mm
	Side 1 55.033mm	-
Innermost track radius (track		
79/39)	Side 0 36.248mm	36.513mm
	Side 1 34.131mm	
Positioning accuracy:	Less than +/- specified test di	•

2.5 Magnetic Head

All types.

Magnetic head:

Read/write head track width: Effective track width after

tunnel erase:

Erase head track width:

Read/write-erase gap spacing:

Read/write gap azimuth:

Gimbal supported read/write head with tunnel erase

o 140

0.160mm nominal

0.150 +/- 0.015mm 0.100mm nominal 0.85 +/- 0.05mm

0° +/- 18' with specified test

disk

Detailed Description and Servicing Disk Drives



2.6 Track Seek Mechanism

All types.

Head positioning mechanism:

Stepping motor:

Stepping motor drive:

Outer/inner stopper: Track 00 detection:

Track to track time:

Settling time:

Average track access time:

Band positioner

4-phase, 200 steps per rev

1 step per track

Mechanical moving stopper LED and photo-transistor

Less than 3msec

Less than 15msec (excluding

track to track time

94msec (including settling

time)

2.7 Head Load Mechanism

All types.

Head load mechanism:

Head load time:

File protect mechanism:

Window margin (shipping):

Plunger solenoid Less than 35msec

Detection of write enable notch

by LED and photo-transistor

More than 600nsec, with specified test disk, MFM method, PLO separator, and 0

write pre-compensation





Detailed Description and Servicing Disk Drives

3 JUMPERS

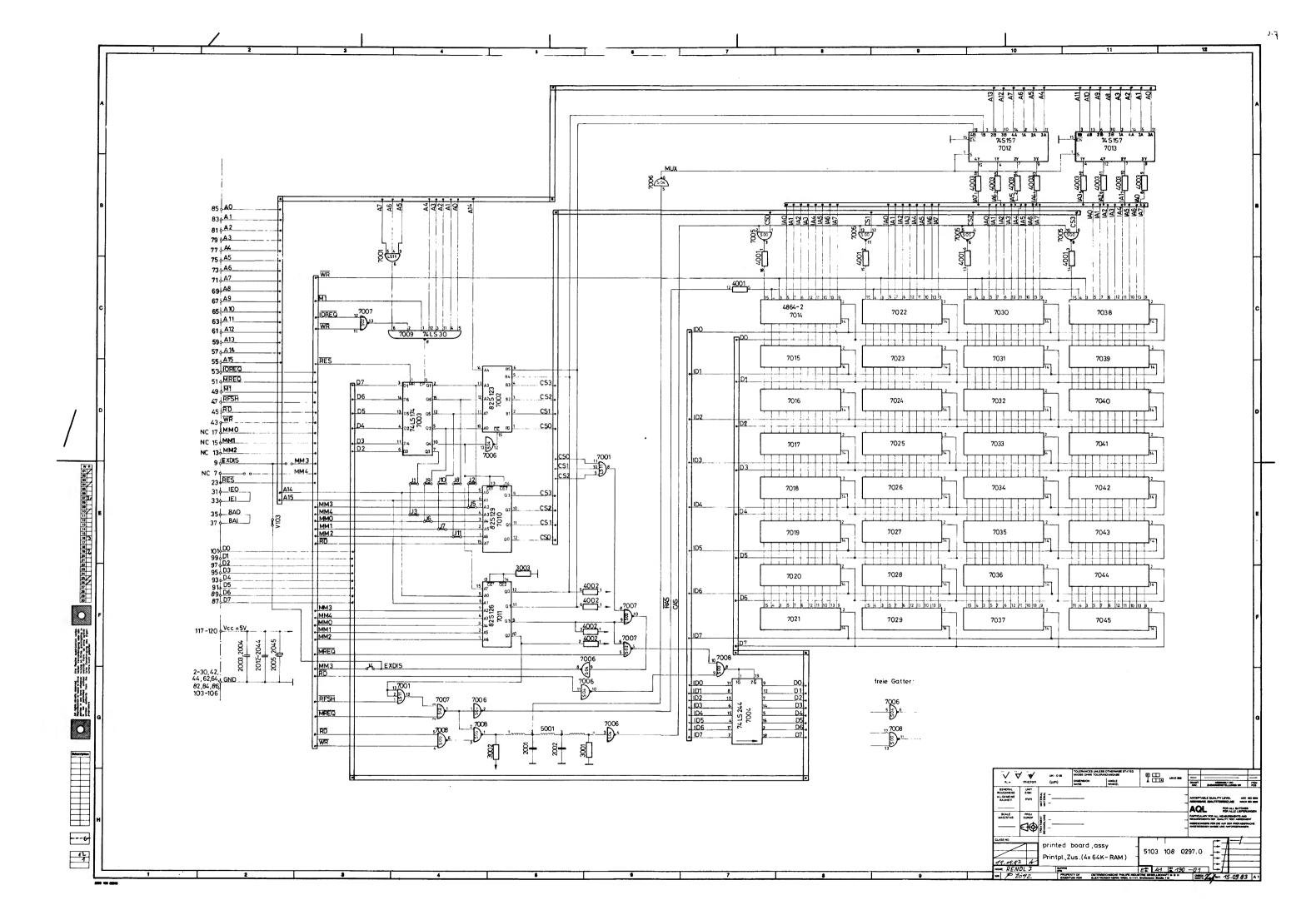
The jumpers required for the various drives are shown below:

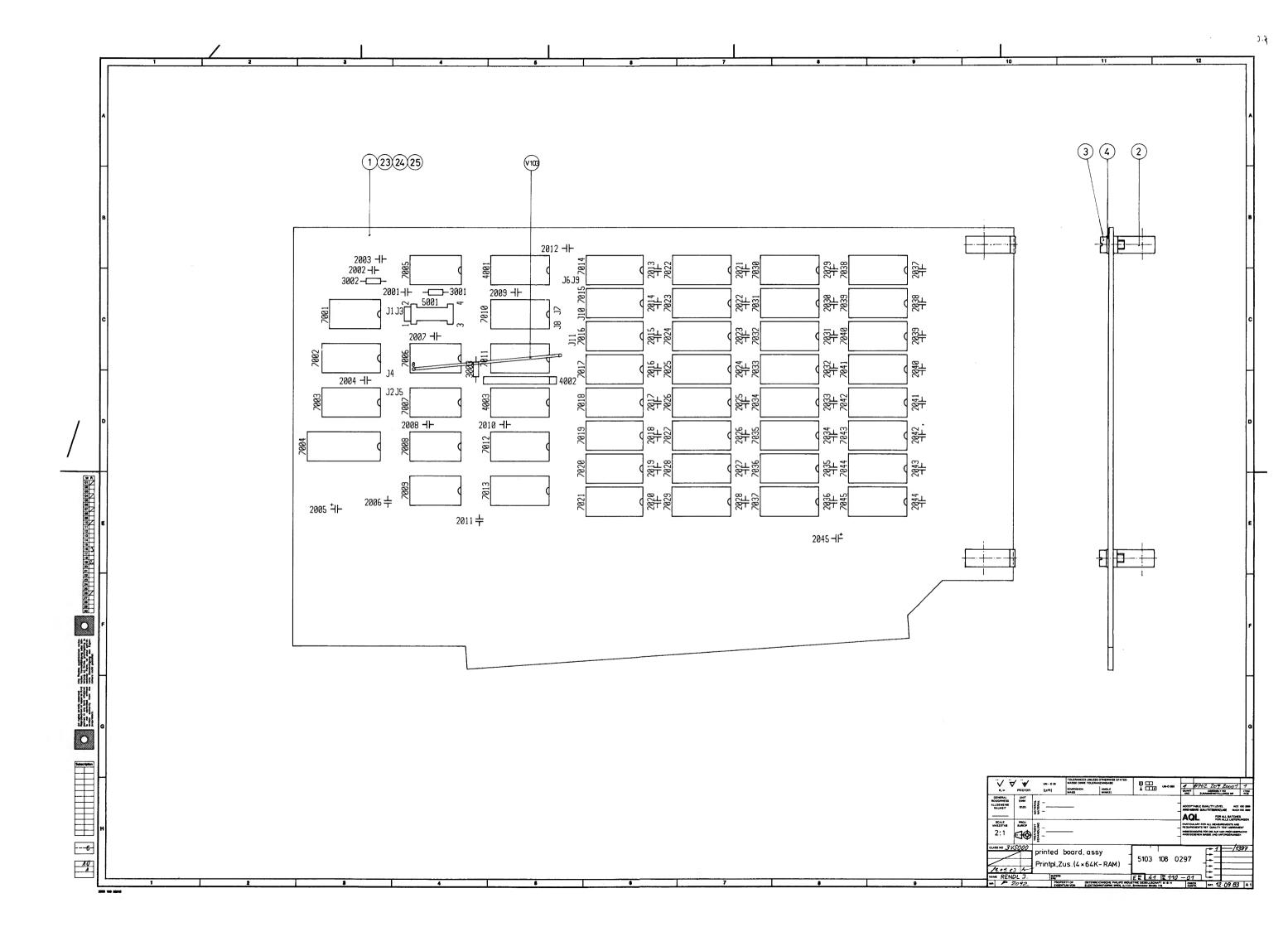
	FD 55A	FD 55F	FD 55A(L)	FD 55F(L)
DS	ST	WT		_
HM	yes	yes	yes	yes
DSO-DS3	yes	yes	yes	yes
MX	no	no	no	no
HS	no	no	no	no
PM	_	_	yes	yes
UR	-	-	no	no
ML	***	-	no	no
IU	_	-	no	no
HL	-	-	no	no
UO	-	_	no	no
U1	_	-	no	no
RE	-	_	no	no
SM	-	_	yes	yes

Detailed Description and Servicing
Disk Drives



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2

Detailed Description and Servicing P2000C Options - Memory Extension P2092

1 GENERAL

The P2000C Memory Extension option provides the user with an additional 256K bytes of RAM, which may be used as RAM Floppy (or cache-memory). Presence of the PCB must be indicated with the use of the Configuration Program if it is to be used as RAM Floppy.

The PCB occupies the extension socket on the Mainboard and instructions for fitting it are given in Part 4 of this manual.

When the Memory Extension is fitted, bank switching functions are carried out by the memory manager on the extension board.

CIRCUIT DESCRIPTION

The 256K bytes of extension memory are made up of 4 banks of 8 dynamic 4864-2 RAM's (items 7014 to 7045), which are divided into 16 segments of 16K bytes and can be selected by a decoder programmed as an output port, which also uses the memory manager signals. The memory images shown in figures 7.1 to 7.7 are possible. The values required to achieve a particular memory configuration (to be output to port FF) are given in the form "FF:=XXH". The values within the memory maps represent the BANK/SEGMENT numbers.

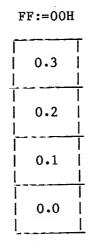


Figure 7.1 Basic Memory Configuration





Extension Memory Arrangement 2.1

The relationship between the Extension Memory, the Main Memory and the various modes is shown in table 7.1.

Standard Bank Switching 2.2

When not using the Memory Extension as RAM Floppy, the Standard Bank Switching Modes (MP/M, OASIS, CROMIX and WRITE ALL) are available to the user (see figures 7.3 to 7.6). These make available the sixteen segments of 16 kbytes of RAM in a variety of configurations.

to these configurations by passing the Access is made appropriate value to output port FF.

2.3 Cache Memory

In Cache Mode, the user has available 15 additional banks of memory, each covering 16 kbytes, as shown in figure 7.7. Each individual bank can be accessed by addressing the bank with:

OUT (FF), A

where A = the value to be sent to output port FF (18H, 28H...F8H).

As shown in figure 7.7, certain memory locations are shared. This gives the Cache Memory the following properties:

- for each of the 15 memory banks, the lower addresses (from 0000H to 3FFFH) are common, allowing data to be effectively 'carried over' to different programs. This area is used as the directory area when the RAM Floppy is implemented.
- for each of the 15 memory banks, the upper addresses (from COOOH to FFFFH) are part of the main memory, allowing data to be 'carried over' to and from main memory routines.
- for each of the 15 memory banks, the addresses from 8000H to BFFFH do not exist and any attempted access to these while in the Cache Mode will give undefined addresses results.
- for each of the 15 memory banks the 16 kbytes between 4000H and 7FFFH are available to the user. These areas are used to store files when the RAM Floppy is implemented.





FF:=90H	FF:=AOH	FF:=BOH	FF:=COH	FF:=DOH	FF:=EOH
1.3	2.3	3.3	4.3	1.0	4.0
1.2	2.2	3.2	4.2	2.0	
1.1	2.1	3.1	4.1	3.0	
0.0	0.0	0.0 0.1	0.0	0.3	0.0

Figure 7.4 5.25 Additional Banks - Using OASIS Switch Mechanism

FF:=94H	FF:=A4H	FF:=B4H	FF:=C4H
1.3	2.3	3.3	4.3
1.2	2.2	3.2	4.2
1.1	2.1	3.1	4.1
1.0	2.0	3.0	4.0

Figure 7.5 4 Additional Banks - Using CROMIX Type Bank Switching





FF:=90H	FF:=AOH	FF:=BOH	FF:=COH	FF := DOH	FF:=EOH
1.3	2.3	3.3	4.3	1.0	4.0
1.2	2.2	3.2	4.2	2.0	
1.1	2.1	3.1	4.1	3.0	
0.0	0.0	 0.0 	0.0	0.3	0.0

Figure 7.4 5.25 Additional Banks - Using OASIS Switch Mechanism

FF:=94H	FF:=A4H	FF:=B4H	FF:=C4H
1.3	2.3	3.3	4.3
1.2	2.2 1	3.2	4.2
1.1	2.1	3.1	4.1
1.0	2.0	3.0	4.0

Figure 7.5 4 Additional Banks - Using CROMIX Type Bank Switching



Extension Memory Arrangement 2.1

The relationship between the Extension Memory, the Main Memory and the various modes is shown in table 7.1.

Standard Bank Switching 2.2

When not using the Memory Extension as RAM Floppy, the Standard Bank Switching Modes (MP/M, OASIS, CROMIX and WRITE ALL) are available to the user (see figures 7.3 to 7.6). These make available the sixteen segments of 16 kbytes of RAM in a variety of configurations.

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Cache Memory 2.3

In Cache Mode, the user has available 15 additional banks of memory, each covering 16 kbytes, as shown in figure 7.7. Each individual bank can be accessed by addressing the bank with:

OUT (FF), A

where A = the value to be sent to output port FF (18H, 28H...F8H).

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- for each of the 15 memory banks, the lower addresses (from 0000H to 3FFFH) are common, allowing data to be effectively 'carried over' to different programs. This area is used as the directory area when the RAM Floppy is implemented.
- for each of the 15 memory banks, the upper addresses (from COOOH to FFFFH) are part of the main memory, allowing data to be 'carried over' to and from main memory routines.
- for each of the 15 memory banks, the addresses from 8000H to BFFFH do not exist and any attempted access to these while in the Cache Mode will give undefined addresses results.
- for each of the 15 memory banks the 16 kbytes between 4000H and 7FFFH are available to the user. These areas are used to store files when the RAM Floppy is implemented.



Detailed Description and Servicing P2000C Options - Memory Extension P2092

1 GENERAL

The P2000C Memory Extension option provides the user with an additional 256K bytes of RAM, which may be used as RAM Floppy (or cache-memory). Presence of the PCB must be indicated with the use of the Configuration Program if it is to be used as RAM Floppy.

The PCB occupies the extension socket on the Mainboard and instructions for fitting it are given in Part 4 of this manual.

When the Memory Extension is fitted, bank switching functions are carried out by the memory manager on the extension board.

2 CIRCUIT DESCRIPTION

The 256K bytes of extension memory are made up of 4 banks of 8 dynamic 4864-2 RAM's (items 7014 to 7045), which are divided into 16 segments of 16K bytes and can be selected by a decoder programmed as an output port, which also uses the memory manager signals. The memory images shown in figures 7.1 to 7.7 are possible. The values required to achieve a particular memory configuration (to be output to port FF) are given in the form "FF:=XXH". The values within the memory maps represent the BANK/SEGMENT numbers.

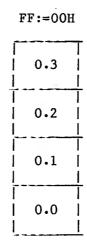
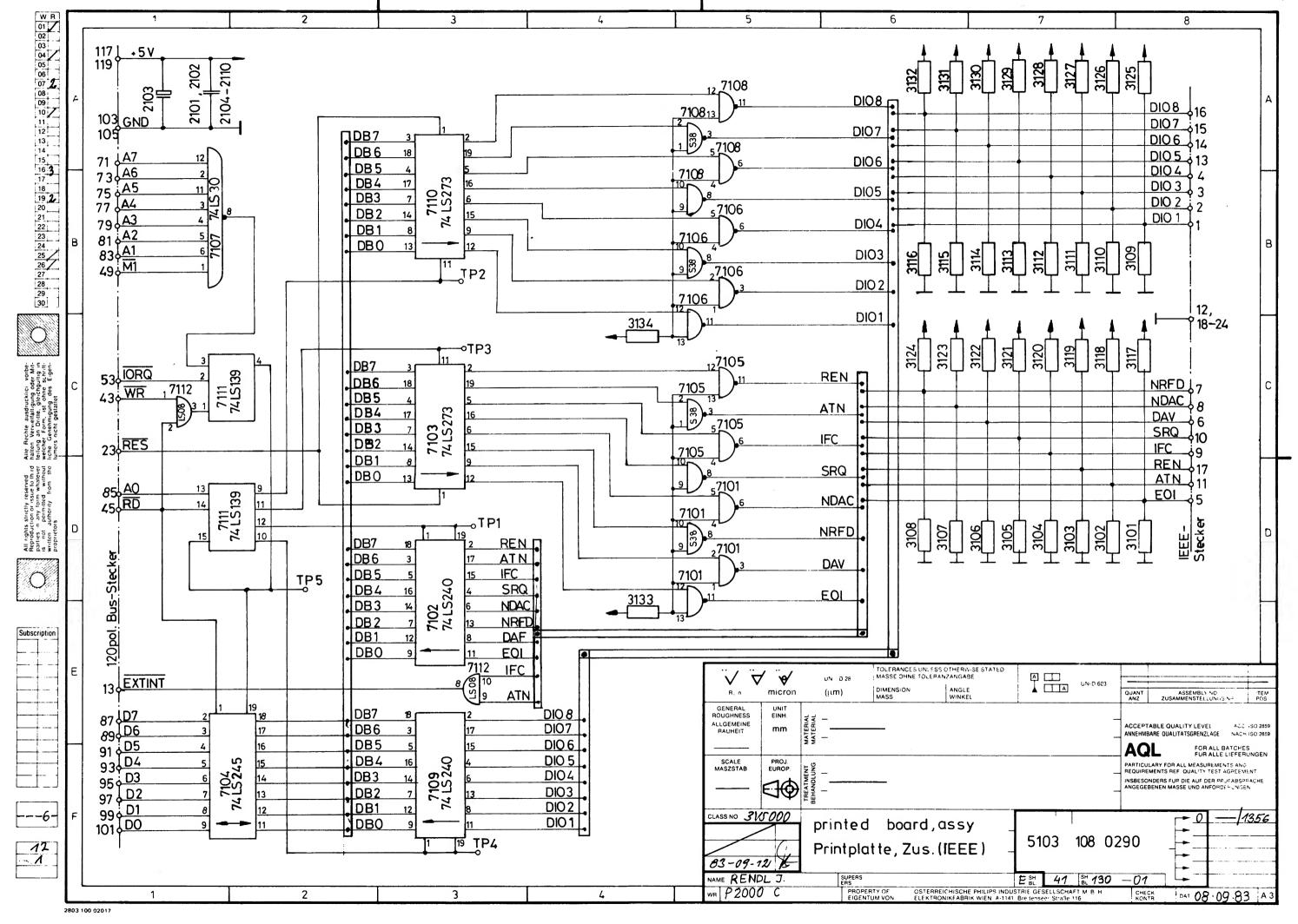


Figure 7.1 Basic Memory Configuration







1 GENERAL

The P2000C IEEE Extension P2091 represents a low cost, degraded version of the Standard Digital Interface for Programmable Instrumentation to the IEEE Std 488-1975, and deals with the interconnection of programmable electronic measuring devices under the control of the P2000C.

The main properties of the P2000C IEEE Extension are as follows:

- Connection of up to 15 devices (in addition to the P2000C)
- A maximum overall distance between P2000C and the furthest device of 20 metres
- Byte serial data transfer dependent on software
- Multiplexing of addresses, commands and data
- 16 bus lines (8 data, 8 control 3 for bus transfer, 5 for bus management)
- Standard codes for addresses and commands (ASCII or ISO 7 bit code)
- Transparent data transfer
- Asynchronous communication (handshake)
- Different baudrates permitted for various devices
- Low cost
- Many devices available with IEEE interfaces

Application:

- Ideal for simple instrumentation systems at medium data rates and over short distances.

This chapter describes the hardware used to provide the digital interface facility. Control of the IEEE Extension board is by software, and is described in the relevent software documentation.

Detailed Description and Servicing P2000C Options - IEEE Extension P2091



1.1 IEEE Bus Signals

The IEEE Bus Signals are defined as follows:

Eight interface signal lines (active-low), carrying all 7 bit interface messages and the device dependent messages.

- DIO1 to DIO8 (data input output 1) to (data input output 8)

Three interface signal lines, used to transfer each byte of data on the DIO signal lines from an addressed talker to all addressed listeners.

- DAV (data valid) indicates the condition (availability and validity) of information on the DIO signal lines.
- NRFD (not ready for data) indicates that the device(s) is(are) not ready/ready to accept data.
- NDAC (not data accepted) indicates that data has been not accepted/accepted by the device(s).

The DAV, NRFD and NDAC signal lines operate in a three-wire (interlocked) handshake process to transfer each data byte across the interface. A timing diagram and description of this process is given in section 4.

Five interface signal lines are used to manage the flow of information across the interface.

- ATN (attention) is used to specify how data on the DIO signal lines are to be interpreted and which device must respond to the data.
- IFC (interface clear) is used to place the interface system, parts of which are contained in all interconnected devices, in a known quiescent state.
- SRQ (service request) is used by a device to indicate the need for attention and to request an interruption of the current sequence of events.
- REN (remote enable) is used (in conjunction with other messages) to select between two alternate sources of device programming data.
- EOI (end or indentify) is used to indicate the end of a multiple byte transfer sequence or, in conjunction with ATN, to execute a polling sequence.



Detailed Description and Servicing P2000C Options - IEEE Extension P2091

2 BLOCK DIAGRAM

Figure 8.1 shows the block diagram of a typical instrumentation system, showing the capability of handling a variety of instrumentation requirements.

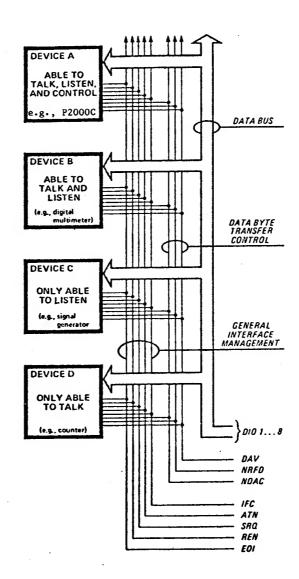


Figure 8.1 Typical Instrumentation System Using IEEE - Block Diagram

Detailed Description and Servicing P2000C Options - IEEE Extension P2091



3 SPECIFICATION

The purpose of the IEEE board is to route signals between the P2000C and the various programmable devices, which will be connected to the Unit Under Test (UUT). These signals are used (typically) to:

- select an appropriate stimulus device
- set the output of the stimulus device
- select an appropriate measurement device
- set the range/mode of the measurement device
- pass the resultant measurement to the CPU for evaluation

This program controlled procedure will be repeated until the condition of the UUT is determined.

The IEEE Extension is built around a 16 bit parallel input/output port (output latched).

3.1 Port Addresses

R/W DIO1 - DIO8 - port address FF R/W Control bus - port address FE

	Control Bus	Data Bu	S
bit0	EOI	DIO1	
bitl	DAV	DIO2	
bit2	NRFD	DIO3	
bit3	NDAC	DI04	
bit4	SRQ	DIO5	
bit5	IFC	DIO6	(INT)
bit6	ATN	DIO7	(INT)
bit7	REN	DIO8	•

3.2 IEEE Interrupt

The interrupt circuit is used to indicate the high to low transition of signals IFC or ATN, using a free Z80-CTC channel to generate a Z80 interrupt (mode2). It is the responsibility of the software to correctly interperate the interrupt. The interrupt address is FFDCH.





3.3 Connection to Mainboard

The following connections to the 120 pin Bus Extension are used by the IEEE board:

Pin	Signal	Direction	Pin	Signal	Direction
13	EINT-N	IN	81	AB2	OUT
23	RES	OUT	83	AB1	OUT
43	WRB-N	OUT	85	ABO	OUT
45	RDB-N	OUT	87	D7	BI
49	M1B-N	OUT	89	D6	BI
53	IORQB-N	OUT	91	D5	BI
71 .	AB7	OUT	93	D4	BI
73	AB6	OUT	95	D3	BI
75	AB5	OUT	97	D2	BI
77	AB4	OUT	99	D1	BI
79	AB3	OUT	101	DO -	BI

Pins 103, 105 are connected to GND Pins 117, 119 are connected to +5V All other odd pins are not connected All even pins 2 - 106 are not connected

The data bus is buffered.

3.4 IEEE Bus

One transceiver circuit is reserved for each bus line. All transceivers are open collector, driving 48mA maximum. The receivers have TTL inputs with hysteresis. Each signal line is locked with two resistors, 3kOhm to +5V and 6.2kOhm to ground. A logic one (high) on the system bus forces a logic true (low) on the IEEE bus. Activating port FE, bit 5 or 6, causes an immediate interrupt.

Detailed Description and Servicing P2000C Options - IEEE Extension P2091



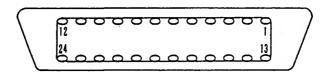
3.5 External Connections

The external IEEE Extension connections are as follows:

Pin	Signal	Pin	Signal
1	DIO1	13	DI05
2	DIO2	14	DIO6
3	DIO3	15	DI07
4	DIO4	16	DIO8
5	EOI	17	REN
6	DAV	18	GND, (6)
7	NRFD	19	GND, (7)
8	NDAC	20	GND, (8)
9	IFC	21	GND, (9)
10	SRQ	22	GND, (10)
11	ATN	23	GND, (11)
12	Shield	24	GND, (Logic)

3.5.1 MOUNTING

Pin designation of the IEEE Extension connector is as shown below, using connector CHAMP AMP No. 552791-2:



3.5.2 CIRCUIT DIAGRAM

For the circuit diagram of the IEEE board P2091, please refer to the main circuit diagrams.



Detailed Description and Servicing P2000C Options - IEEE Extension P2091

4 CIRCUIT DESCRIPTION

4.1 IEEE Selection

The IEEE board is selected by the use of Address lines A1 to A7 and the signal M1-N, via a gate (item 7107). The output of this gate is multiplexed (items 7111/7112) with the signals IORQ-N, WR-N, RD-N and Address line A0 to produce the chip select signals for the output latches and input buffers.

4.2 IEEE Output

Information (in the form of data or control signals) is held in the bi-directional latch (item 7104). The two output latches (items 7103/7110) will feed this information onto either the IEEE data lines or control lines, depending on the chip select signal, via open collector drivers (items 7101/7105/7106/7108).

4.3 IEEE Input

Information returned from the external instrumentation system is buffered and fed (via item 7104) to the P2000C data bus. The selection between the data buffer (item 7109) and the control buffer (item 7102) is determined by the chip select signal. An external interrupt (EXTINT-N) is generated when signal lines IFC (Interface Clear) and ATN (Attention) are active, via item 7112.

4.4 Line Termination

All 16 lines are terminated, on the IEEE board, with 3k to 5V and 6.2k to ground.

4.5 Test Points

Five test points are available (TP1 to TP5) on the IEEE board, giving access to the chip select signals for the board and the data and control input/output devices.

Detailed Description and Servicing P2000C Options - IEEE Extension P2091



4.6 Handshake Timing

The handshake process is used to control the transfer of all data between talker and listener.

Figure 8.2 shows this process by illustrating the waveforms on the DAV, NRFD and NDAC signal lines. NRFD and NDAC represent composite signals where two or more listeners accept the same data byte at slightly differing times. The annotated numbers on the timing diagram are explained below.

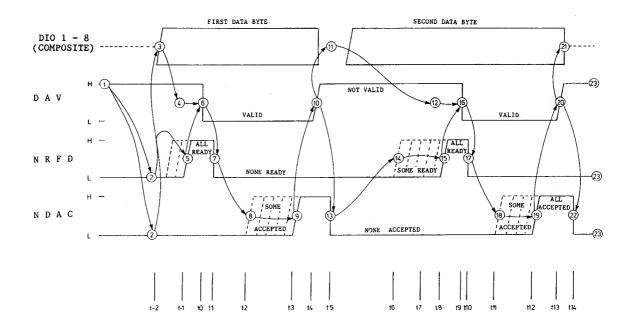


Figure 8.2 IEEE Extension - Handshake Timing

(1)		Source initializes DAV to high (H) (data not valid).
(2)		Acceptors initialize NRFD to low (L) (none are ready for data), and set NDAC to low (L) (none have accepted the data).
(3)	t-2	Source checks for error condition (both NRFD and NDAC high), then sets data byte on DIO lines.
(4)	t-2 to t0	Source delays to allow data to settle on DIO lines.
(5)	t-1	All acceptors have indicated readiness to accept first data byte: NRFD goes high.
(6)	t0	When source senses NRFD high it sets DAV low to indicate valid and settled data on line.





Detailed Description and Servicing P2000C Options - IEEE Extension P2091

(7) tl	First acceptor sets NRFD low to indicate that it is no longer ready, then accepts the data.
	Other acceptors follow at their own rates.
(8) t2	First acceptor sets NDAC high to indicate that
•	it has accepted the data. (NDAC remains low due
	to other acceptors).
(9) t3	Last acceptor sets NDAC high to indicate that
()) =3	it has accepted data, and line goes high.
(10) t4	Source senses NDAC high, sets DAV high. This
(10) 64	indicates to acceptors that data on DIO lines
	can no longer be considered valid.
(11) t4 to t7	Source changes data on the DIO lines.
	Source delays to allow data to settle on the
(12) t7 to t9	DIO lines.
(12) 45	
(13) t5	
	low in preparation for next cycle. NDAC goes low as the first acceptor sets the line low.
(1/) +6	First acceptor indicates that it is ready for
(14) t6	
	next data byte by setting NRFD high. (NRFD
	remains low due to other acceptors not yet
(15) .0	ready).
(15) t8	Last acceptor indicates that it is ready for
	the next data byte by setting NRFD high: NRFD
(1 ()) ()	signal line goes high.
(16) t9	Source senses NRFD high and sets DAV low to
	indicate valid and settled data on DIO lines.
(17) t10	First acceptor sets NRFD low to indicate that
	it is no longer ready, then accepts the data.
(18) t11	First acceptor sets NDAC high to indicate that
	it has accepted the data as in (8).
(19) t12	Last acceptor sets NDAC high to indicate that
	it has accepted the data as in (9).
(20) t13	Source senses NDAC high, sets DAV high as in
	(10).
(21)	Source removes data byte from DIO signal lines
•	after setting DAV high.
(22) t14	Acceptors sense DAV high and set NDAC low in
•	preparation for next cycle.
(23)	Note that all three handshake lines are at
\ - - /	their initialized states as in (1) and (2).
	(2)

Detailed Description and Servicing P2000C Options - IEEE Extension P2091



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Servicing
Removal and Replacement of Assemblies and Units

1 GENERAL

This chapter gives details of the recommended methods of removing and replacing assemblies and units of the P2000C.

WARNING

ALWAYS REMOVE THE MAINS CONNECTOR FROM THE REAR OF THE UNIT BEFORE ATTEMPTING TO REMOVE COVER OR TO CARRY OUT ANY SERVICING ON THE P2000C

2 THE COVER

The cover must be removed to gain access to all assemblies and units of the P2000C.

To remove the cover, first ensure that the:

- power cable is disconnected (safety wait time)
- keyboard and any other peripherals are disconnected
- diskettes are removed (from drives and storage compartment)
- carrying strap is removed

Remove the four screws labelled (A) in View 1. Carefully remove the cover, taking care not to damage any of the screening springs.

Before refitting the cover, make sure that all wiring is in good order and cannot become trapped.

Servicing Removal and Replacement of Assemblies and Units



The following paragraphs assume the cover to be removed, and describe removal and refitting of:

- Terminalboard
- Mainboard
- flexible disk drives
- monitor
- power supply unit
- mains switch
- mains socket
- distribution board
- keyboard cable assembly(internal)
- optional boards (IEEE or RAM-BOARD)

3 MAINBOARD AND TERMINALBOARD

These two PCB's are fitted to a sub-chassis, which must be removed to gain access to either board.

If the Mainboard is to be replaced, remove the rear mask as described in 3.2.

Remove the three screws labelled (A) in View 2 and loosen the four screws labelled (A) in View 3.

The sub-chassis can then be withdrawn slightly as shown in View 3, and removed after disconnecting the five mini-match connectors, the connectors to the disk drives and then the sixth mini-match connector.

Reverse the above order when refitting the sub-chassis.

3.1 Terminalboard

Disconnect the link between the two PCB's.

Remove the four retaining screws and lock washers labelled (A) in View 4.

Slide PCB off of retaining lugs and remove.

Reverse the above order when refitting the PCB, not forgetting the lock washers - which also have an electrical bonding function.



Servicing Removal and Replacement of Assemblies and Units

3.2 Mainboard

Disconnect the link between the two PCB's. Remove the six x-point screws labelled (B) in View 2 and remove the rear mask.

Remove the three screws labelled (A) in View 5.

The PCB can then be removed.

Reverse the above order when refitting, ensuring that the lock washer is replaced between the chassis and the earth tags.

FLEXIBLE DISK DRIVES

Remove the strengthening strip by removing the three screws labelled (B) in View 3 and loosening the two screws labelled (C) in View 3.

Ensure that the drive levers are in the closed (down) position. Remove the retaining clips labelled (A) in View 6. Remove the cover plate labelled (B) in View 6. The two drives can then be removed. Disconnect the signal connectors and power connectors as the drives are withdrawn.

The P2000C disk drives are supplied without the locating pins, labelled (A) in View 7. Ensure that these items are removed before returning the drive for servicing.

Reverse the above order when refitting the drives.

4.1 Jumpers and Pull Up Resistors

The P2000C is capable of driving up to four $5\frac{1}{4}$ " disk drives, two internal and two external.

View 7 shows the pull-up resistance network, labelled (B), which must be fitted to the last drive in the chain. If external drives are used, the last drive in the external chain must also be fitted with a pull-up resistance network.

Servicing Removal and Replacement of Assemblies and Units



Drive addresses and head load conditions are selected by the jumpers on the PCB's, as shown in View 7 (labelled C).

Three jumpers must be fitted to each drive: - HM: to select Head Load with Motor On

- DS: DSO - DS3 to define drive number, where:

DSO = Drive 1 DS1 = Drive 2 DS2 = Drive 3 DS3 = Drive 4

- DS(ST/WT): to define the track density, with:

ST for 48tpi WT for 96tpi

This jumper must correspond to the properties of the particular drive.

5 MONITOR

HIGH VOLTAGE WARNING

HIGH VOLTAGES HAVE BEEN USED IN THIS UNIT AND MAY STILL BE PRESENT AFTER SWITCH OFF

Remove the strengthening strip by removing the three screws labelled (B) in View 3 and loosening the two screws labelled (C) in View 3.

Remove the F/D power cable from the clips at the rear of the monitor, labelled (A) in View 8.

Disconnect the video connector at the rear of the monitor, labelled (B) in View 8.

Remove the two screws labelled (D) in View 3.

Lift the monitor out, taking care not to damage the surrounding wiring.

Reverse the above order when refitting the monitor, noting the locating pins close to the two fixing points. Ensure that all cables are replaced in the cable clips.



Servicing Removal and Replacement of Assemblies and Units

6 FRONT MASK

In order to replace the power supply and associated items it is necessary to remove the front mask.

Loosen the four screws labelled (E) in View 3 and remove the screw labelled (B) in View 1. Ease the mask forward and carefully unclip the Power Distribution Panel as shown in View 9 (start with the clip

nearest the power LED).
The mask is then free.

Reverse the above order when refitting the front mask.

7 POWER SUPPLY UNIT

Remove the strengthening strip by removing the three screws labelled (B) in View 3 and loosening the two screws labelled (C) in View 3.

Remove the front mask as described in paragraph 6.

Loosen the two screws labelled (F) in View 3, and lift the unit out of its supports. Remove the two connectors.

Reverse the above order when refitting the power supply unit, ensuring that the unit is firmly seated in the support lugs labelled A in view 11 and that the wiring will be clear of the distribution board.

7.1 Fuse Replacement

It is necessary to remove the power supply unit to gain access to the fuse holder.

Servicing Removal and Replacement of Assemblies and Units



MAINS SWITCH 8

Remove the Power Supply Unit as described in paragraph 7.

Remove the switch cap.

Remove the upper two screws labelled (B) in View 11, which hold the switch to the bracket.

Note: The two lower screws are preset to align the switch with the front mask and should not need adjusting.

Unsolder the switch connections.

Reverse the above order when refitting the switch.

MAINS SOCKET 9

Remove the Power Supply Unit as described in paragraph 7. Unsolder the mains socket connections. in view 11 securing the Remove the two screws labelled (C) socket and the earth tag labelled (D) in view 11.

Reverse the above order when refitting the socket.

DISTRIBUTION PANEL 10

Remove the Monitor as described in paragraph 5. Remove the Power Supply Unit as described in paragraph 7. Disconnect the Distribution Panel connectors.

Reverse the above order when refitting the Distribution Panel.

KEYBOARD CABLE ASSEMBLY (INTERNAL) 11

Remove the front mask as described in paragraph 6. The removal of the cable assembly will be simplified by the removal of the Monitor as described in paragraph 5. Remove the cable strap labelled (E) in View 11. Remove the two screws labelled (F) in View 11. Pass the keyboard socket inside the P2000C and disconnect the other end from the Terminalboard (7 way mini-match connector).

Reverse the above order when refitting the Keyboard Cable Assembly, ensuring that a new cable strap is fitted.



Servicing Removal and Replacement of Assemblies and Units

12 TILT-BAR

Remove the six screws labelled (C) and the single screw labelled (B) in View 1.

Ease off the bottom plate.

The tilt-bar can now be removed.

Reverse the above order when refitting the tilt-bar.

13 OPTIONAL PCB's (IEEE OR RAM FLOPPY)

One of two optional PCB's may be fitted to the extension Mainboard. The following procedure is connector on the recommended for fitting these boards:

Remove the sub-chassis as detailed in paragraph 3.

Remove the strengthening strip by removing the three screws labelled (B) in View 3 and loosening the two screws labelled (C) in View 3.

Remove the Monitor as detailed in paragraph 5.

Fit the optional board into the extension socket on the Mainboard.

- In the case of the IEEE board, the blanking plate labelled (B) in View 5 will be replaced with the IEEE socket plate.
- In the case of the RAM FLOPPY board, the brackets on the PCB must be fixed by two screws to the blanking plate.

Replace the sub-chassis, using the slots in the underside of the cable clamps to locate the top of the optional board as shown in View 10, and remake all connections.

Note: Extreme care must be taken to protect components on the board when refitting a sub-chassis which incorporates an optional PCB.

Refit the Monitor, strengthening strip and cover.

Servicing Removal and Replacement of Assemblies and Units



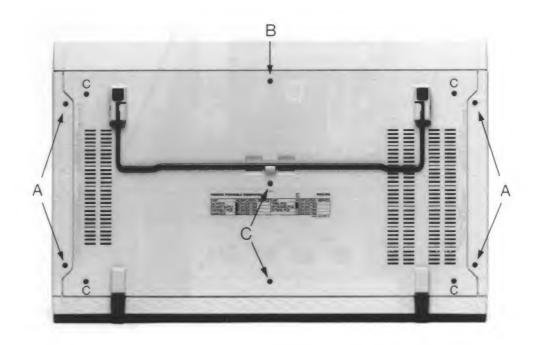
14 KEYBOARD

The keyboard contains one PCB, which holds the keyboard electronics and the keys. To gain access to the PCB, remove the three screws from the back of the keyboard housing and remove the top-cover.

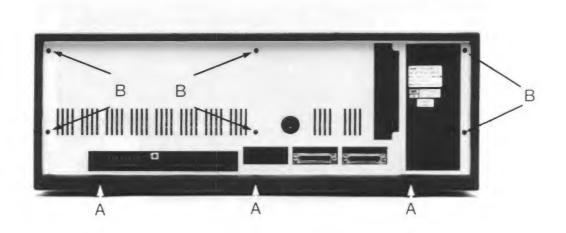
This may be achieved by pressing down firmly on the three points labelled (X) in View 12 (one at a time) with the thumb. At the same time, lift the front of the keyboard top-cover with the finger-nails and ease the back of the top-cover up slightly and pull backwards with the other hand. The pressure applied to the casing must be in a curving movement from front to back of the unit. The PCB is secured by a groove in the front and two screws at the back.

Reverse the above order when refitting the cover, ensuring that the keyboard connector is correctly positioned. When refitting the PCB, ensure that it is firmly seated in the locating groove.





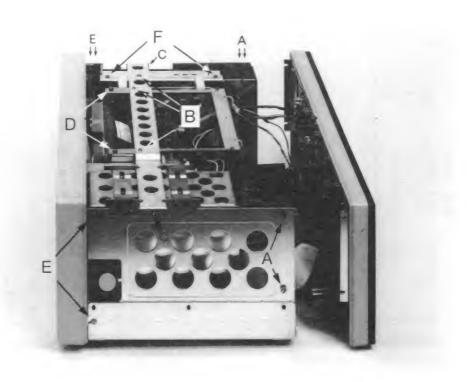
P2000C Part Replacement - View 1



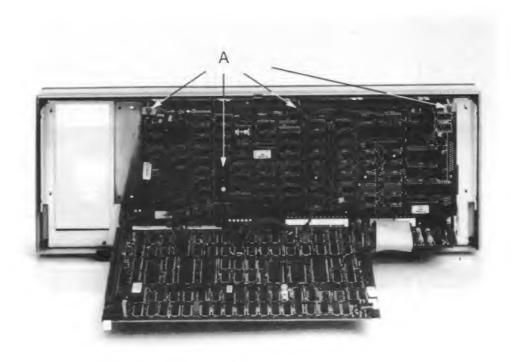
P2000C Part Replacement - View 2

Servicing Removal and Replacement of Assemblies and Units





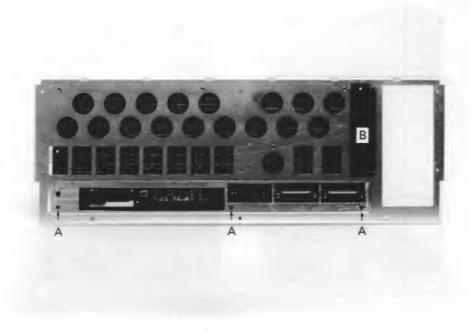
P2000C Part Replacement - View 3



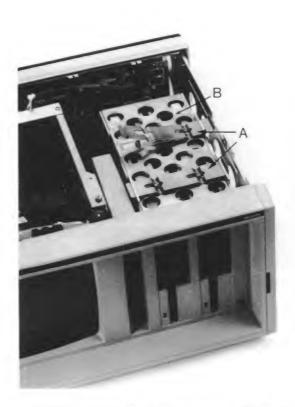
P2000C Part Replacement - View 4



$\begin{array}{c} \textbf{Servicing} \\ \textbf{Removal and Replacement of Assemblies and Units} \end{array}$

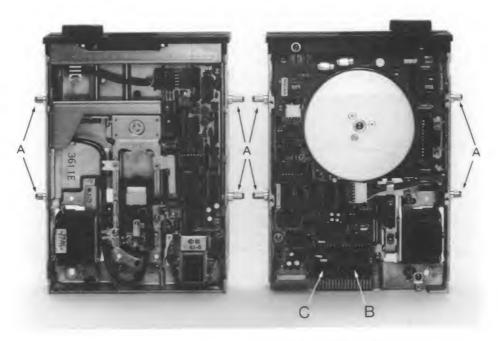


P2000C Part Replacement - View 5

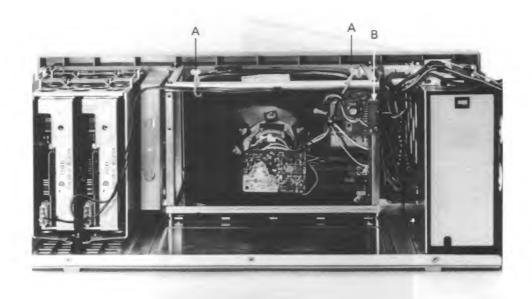


P2000C Part Replacement - View 6





P2000C Part Replacement - View 7



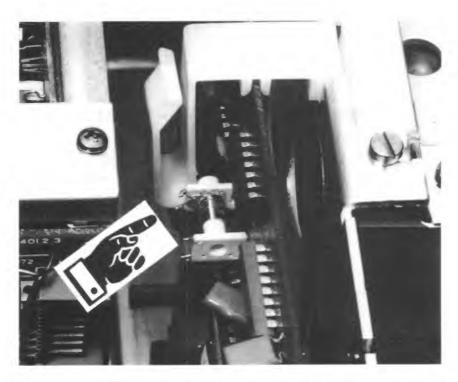
P2000C Part Replacement - View 8



Servicing Removal and Replacement of Assemblies and Units



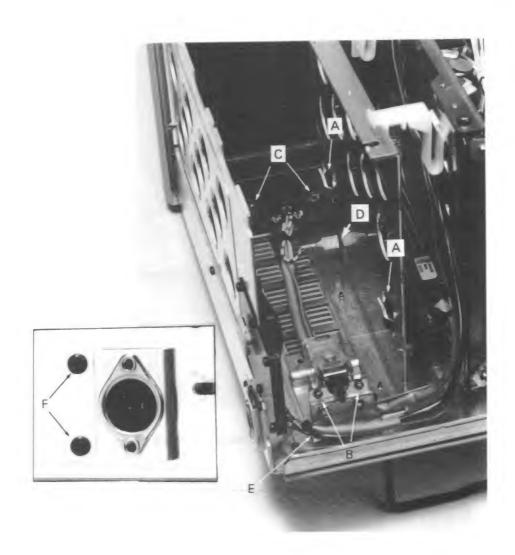
P2000C Part Replacement - View 9



P2000C Part Replacement - View 10

 $\begin{array}{c} \text{Servicing} \\ \text{Removal and Replacement of Assemblies and Units} \end{array}$





P2000C Part Replacement - View 11



Servicing Removal and Replacement of Assemblies and Units



P2000C Part Replacement - View 12



P2000C Part Replacement - View 13



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Servicing Component Location

1 GENERAL

The following diagrams show the location of components relating to the functional blocks described in Part 3.

Each diagram will be annotated with the heading and page number of the first page of the section describing it.

Components that are used exclusively for a function are shown with darker shading; the lighter shading indicates partial or peripheral use of the component.

1.1 Mainboard

CPU	4.1 2-3
DMA	4.1 2-3
Data Buffers	4.1 2-4
Clock Generator	4.1 2-4
I/O Decoder	4.1 2-5
Memory Manager	4.1 2-5
Random Access Memory	4.1 2-6
IPL ROM	4.1 2-6
SAS Interface	4.1 2-7
Flexible Disk Controller	4.1 2-7
Baud Rate Generator - CTC	4.1 2-8
Serial Interface	4.1 2-8

1.2 Terminalboard

CPU	4.1 2-9
CRTC	4.1 2-9
Timing	4.1 2-10
RAM Banks	4.1 2-10
Address Multiplexer	4.1 2-11
Data Buffer	4.1 2-11
Shift Register	4.1 2-12
Attribute Mixing	4.1 2-12
Character Generator ROM	4.1 2-13
CTC	4.1 2-13
V24/Internal Interfac	4.1 2-14
Address Decoder	4.1 2-14
Keyboard Logic	4.1 2-15

Detailed Description and Servicing Component Location



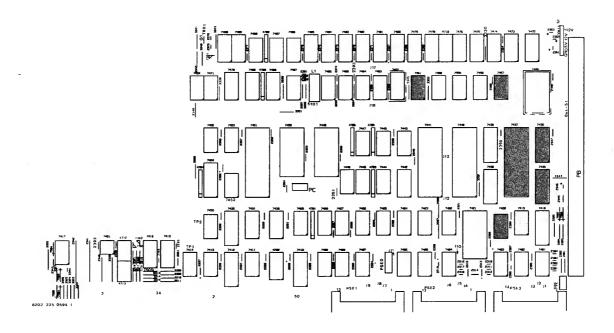
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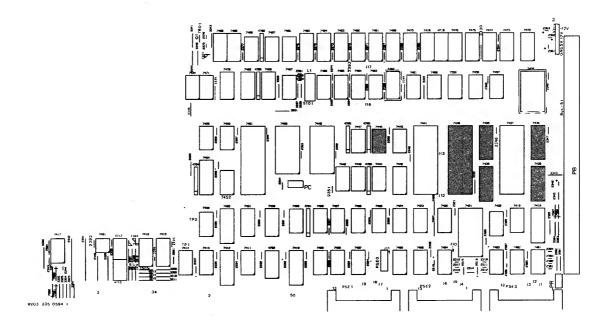


Servicing Component Location

Mainboard - CPU 3.2 / 2-1



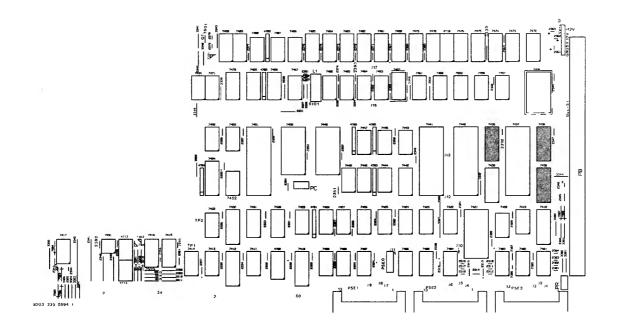
Mainboard - DMA 3.2 / 3-1



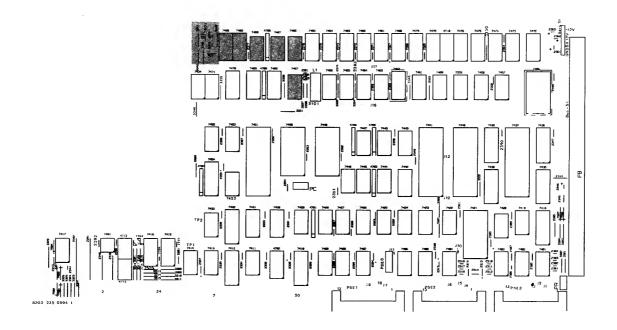
Servicing Component Location



Mainboard - Data Buffers 3.2 / 4-1



Mainboard - Clock Generator 3.2 / 5-1

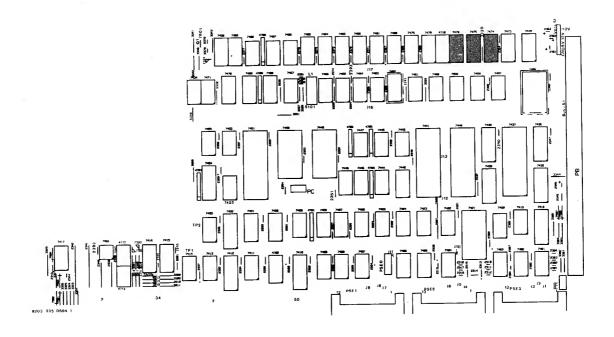




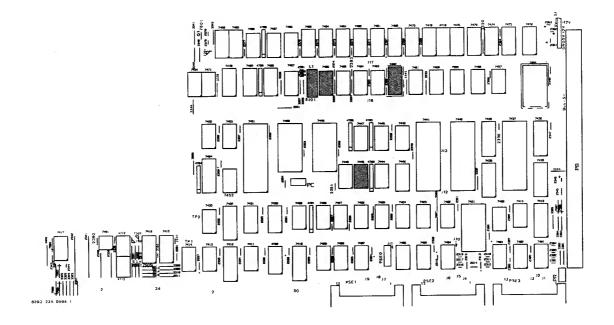


Servicing Component Location

Mainboard - I/O Decoder 3.2 / 6-1



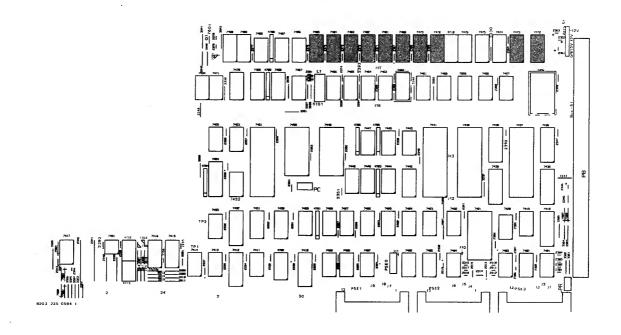
Mainboard - Memory Manager 3.2 / 7-1



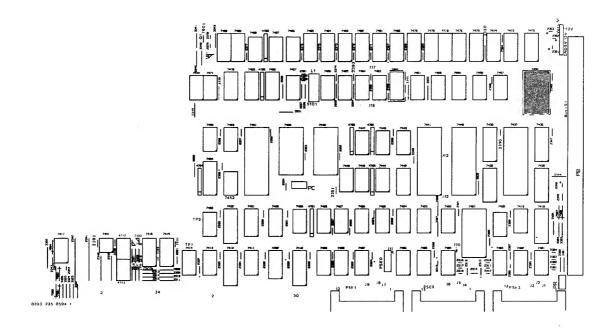
Servicing Component Location



Mainboard - Random Access Memory 3.2 / 8-1



Mainboard - IPL ROM 3.2 / 9-1

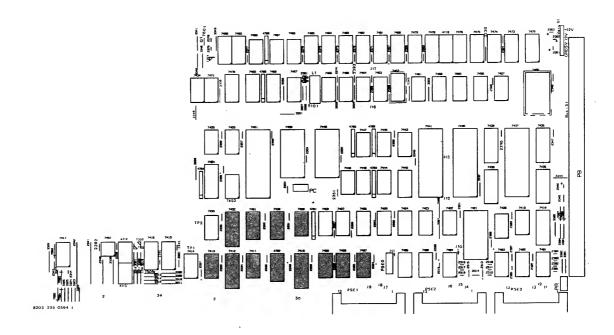




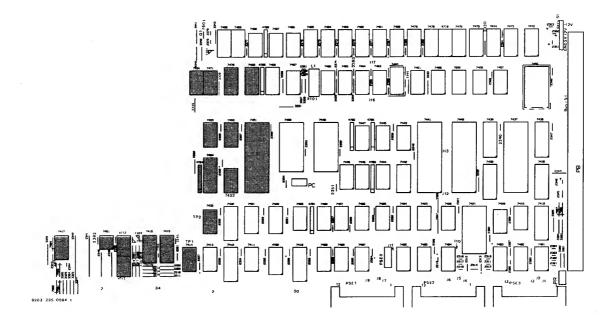


Servicing Component Location

Mainboard - SAS Interface 3.2 / 10-1



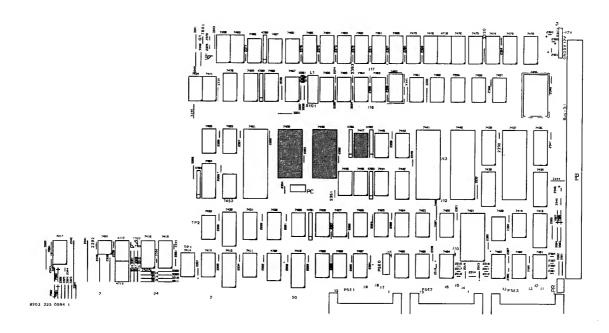
Mainboard - Flexible Disk Controller 3.2 / 11-1



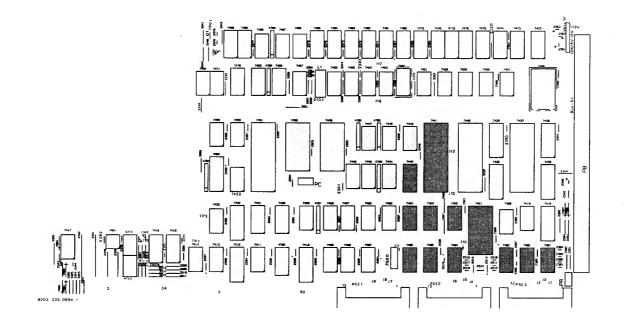
Servicing Component Location



Mainboard - Baud Rate Generator CTC 3.2 / 12-1



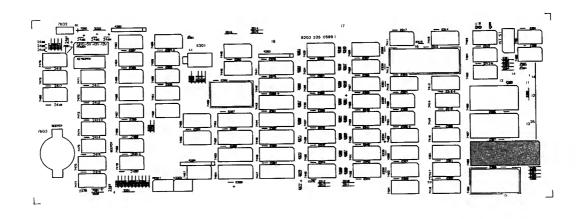
Mainboard - Serial Interfaces 3.2 / 13-1



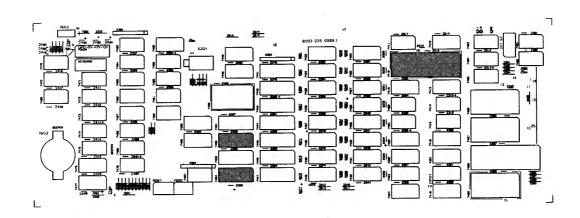


Servicing Component Location

Terminalboard - CPU 3.3 / 2-1



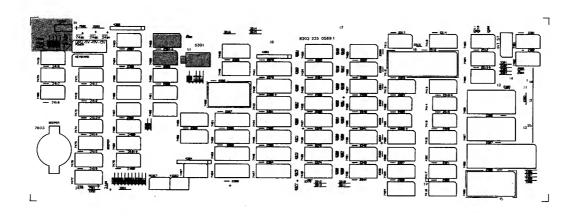
Terminalboard - CRTC 3.3 / 3-1



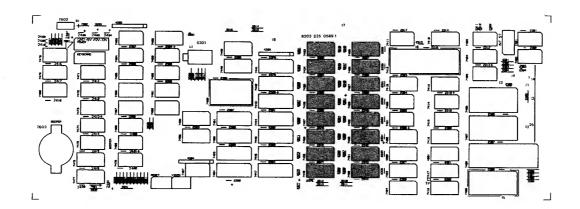
Servicing Component Location



Terminalboard - Timing 3.3 / 4-1



Terminalboard - RAM Banks 3.3 / 5-1

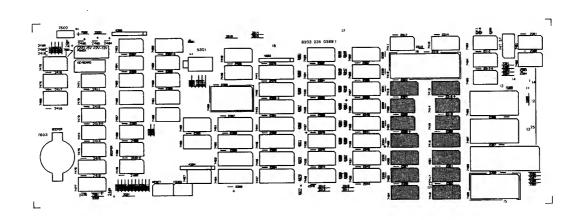




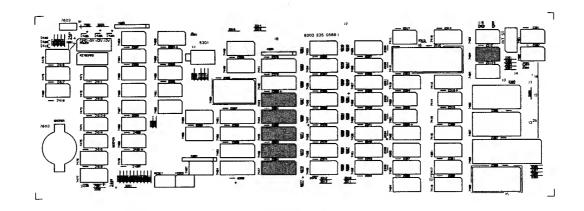


Servicing Component Location

Terminalboard - Address Multiplexer 3.3 / 6-1



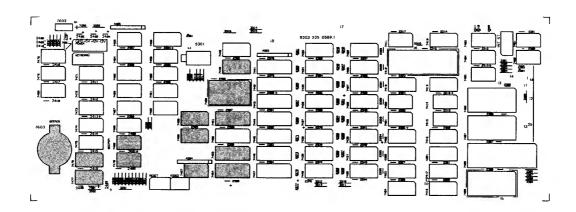
Terminalboard - Data Buffer 3.3 / 7-1



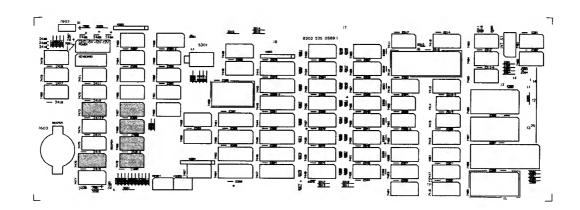
Servicing Component Location



Terminalboard - Shift Register 3.3 / 8-1



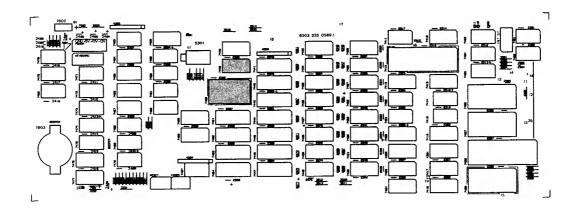
Terminalboard - Attribute Mixing 3.3 / 9-1



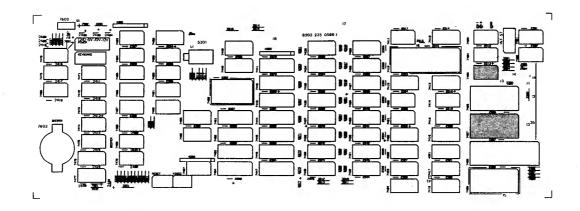


Servicing Component Location

Terminalboard - Character Generator ROM 3.3 / 10-1



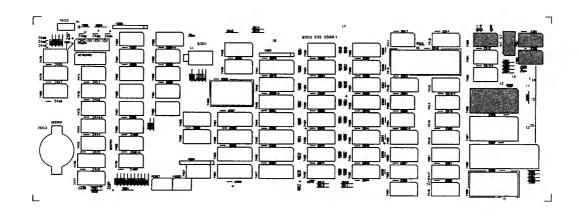
Terminalboard - CTC 3.3 / 11-1



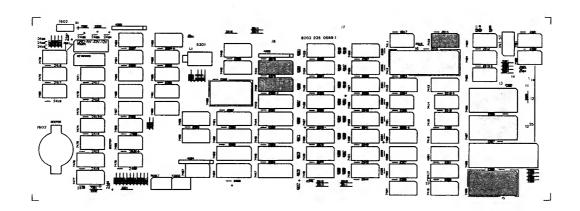
Servicing Component Location



Terminalboard - V24/Internal Interface 3.3 / 12-1



Terminalboard - Address Decoder 3.3 / 13-1

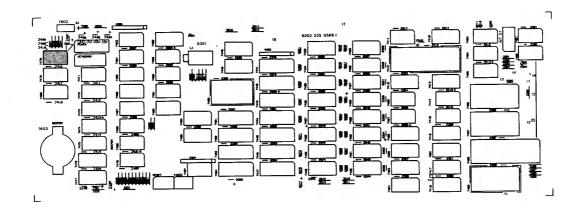






Servicing Component Location

Terminalboard - Keyboard Logic 3.3 /14-1



Detailed Description and Servicing Component Location



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SPARE PART CATALOGUE

1984-04-14

1 GENERAL

This Spare Part Catalogue includes all electrical and the more important mechanical components and parts of the P2000C Portable Computer, covering both P 2010 and P 2012 and Options.

This catalogue is arranged in order of ITEM NUMBER under each heading, where the correct description and the SERVICE CODE of the item will be found.

ITEM part number of component on service print QTY quantity per item number DESCRIPTION .. definition and/or component value CODE NUMBER .. 12NC used in manufacturing SERVICE CODE . 12NC must be used for ordering

Special components and units, which are indicated in the part lists with an "*", are held on stock in the factory in Vienna. All other components are held on stock in the Concern Service

For ordering the following addresses must be used:

for "*" marked components and units:

Osterreichische Philips Ind. G.m.b.H EFW-Microelectronics

Service Department Breitenseerstr. 116

A-1140 W I E N A U S T R I A

Telex: EFPHI 131724

for standard components

in Eindhoven.

Philips Export B.V. Concern Service Building SBP 5

Eindhoven Holland

1983-10-14

SPARE PART CATALOGUE ORDER FORM



1.1 Order Form

If you would like to be kept informed about any updates to this System Reference and Service Manual, please complete the form on the following page and return it to the address indicated.

Please fill in your name and address in CAPITALS.

As each update becomes available you will be informed of its content and of any costs that may be incurred, covering administration and postal charges.

Osterreichische Philips Ind. G.m.b.H EFW-Microelectronics

Service Department Breitenseerstr. 116

 Österreichische Philips Ind. G.m.b.H EFW-Microelectronics

Service Department Breitenseerstr. 116 A-1140 W I E N

A U S T R I A

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Yes.	ı	Want	ĽΟ	nave	tne	upaates	ΕO	Lne

0	Spare	Part	Catalogue	
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o Reference Part

please cross the required updates

- o Complete Manual
- o Price List

and I agree that my name is stored and that I will be informed when relevant information is available.

Surname	:	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Forename	:	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Company	:	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Address																				
Street/no	:	•		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Town/City	:	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Post code	:	•	•		•															
Country	:	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Signature																				





SPARE PART CATALOGUE MAINBOARD

1984-04-14

ITEM	QTY	DESCRIPTION	CODE NUMBER	SERVICE NUMBER
61	1	MAINBOARD PCB ASSY	5103 108 02710	* 5103 109 30000
2	1	SOCKET 8-pin 0-826375-8 (AMP)	2422 025 04093	
3	- 1	SOCKET 6-pin 0-826375-6 (AMP)	2422 038 00122	
4	ī	SOCKET 4-pin 0-826375-4 (AMP)	2422 025 04092	* 5103 109 30400
5	1	CABLE ASSY 34-way 3FD1/2	5103 107 81230	
6	1	SOCKET CONNECTOR 7-pin PRINTER	5103 108 73600	
7	1	SOCKET CONNECTOR 11-pin COMMS.	5103 108 73620	
31	2	IC-SOCKET 40-pin	3103 238 73270	
32	1	IC-SOCKET 24-pin	3103 238 73250	
33	ī	IC-SOCKET 16-pin	5103 108 70200	5322 255 44107
37	1.	CONNECTOR 2 x 60-pin	2422 023 98122	* 5103 109 30390
٠.		•		
2301	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	
2302	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	
2303	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	
2304	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	
2305	1	CER-CAP 100 N S 63 V SI	EM. 2012 572 10028	
2306	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	
2307	1	CER-CAP 100 N S 63 V SI	EM. 2012 572 10028	* 5103 109 30600
2308	1	EL-CAP 4 M 7 63 V	2222 035 38478	
2309	1	CER-CAP 100 N S 63 V SI	EM. 2012 572 10028	* 5103 109 30600
2310	1	CER-CAP CL.1 56 P 100 V	2222 682 34569	
2311	1	CER-CAP CL.1 56 P 100 V	2222 682 34569	
2312	1	CER-CAP CL.1 56 P 100 V	2222 682 34569	
2313	1	EL-CAP 4 M 7 63 V	2222 035 38478	
2314	1	CER-CAP 100 N S 63 V SI	EM. 2012 572 10028	
2315	1	CER-CAP 100 N S 63 V SI	EM. 2012 572 10028	* 5103 109 30600
2320	1		EM. 2012 572 10028	* 5103 109 30600
2321	1	021 011 2 T	EM. 2012 572 10028	
2322	1		EM. 2012 572 10028	
2323	1		EM. 2012 572 10028	
2324	1	EL-CAP 4 M 7 63 V	2222 035 38478	
2325	1		EM. 2012 572 10028	
2326	1		EM. 2012 572 10028	
2327	1		EM. 2012 572 10028	
2328	1		EM. 2012 572 10028	
2329	1	CER-CAP 100 N S 63 V SI	EM. 2012 572 10028	* 5103 109 30600

1983-10-14

SPARE PART CATALOGUE MAINBOARD



ITEM	QTY	DESCRIPTION				CODE	NUMBER	SERV	ICE NUMBER
2330	1	EL-CAP	4 M 7	63 V		2222	035 38478	4822	124 40246
2331	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2332	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2333	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2334	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2335	1	CER-CAP	100 N	S 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2336	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2337	1	EL-CAP	4 M 7	63 V		2222	035 38478	4822	124 40246
2338	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2339	1	PP-CAP	1 N3	G 250 V		2222	457 71302	* 5103	109 30630
2340	1	PP-CAP	1 N3	G 250 V		2222	457 71320		109 30630
2341	1	PP-CAP		G 63 V			455 74703		109 30640
2342	1	PP-CAP	47 N	G 63 V			455 74703		109 30640
2343	1	CER-CAP		s 63 V	SIEM.		572 10028		109 30600
2344	1	CER-CAP		G 100 V			682 28101		109 30540
2345	1	CER-CAP		s 63 V	SIEM.		572 10028		109 30600
2346	1	EL-CAP	4 M 7				035 38478		124 40246
2347	1	CER-CAP		s 63 V			572 10028		109 30600
2348	1	CER-CAP		s 63 V			572 10028		109 30600
2349	1	CER-CAP	100 N	S 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2350	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2351	1	CER-CAP		S 63 V			572 10028		109 30600
2352	1	CER-CAP		s 63 V			572 10028		109 30600
2353	1	CER-CAP		s 63 V			572 10028		109 30600
2354	1	CER-CAP		s 63 V			572 10028		109 30600
2356	1	CER-CAP		s 63 V			572 10028		109 30600
2357	1	CER-CAP		s 63 V			572 10028		109 30600
2358	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2359	1	EL-CAP	4 M 7	63 V		2222	035 38478	4822	124 40246
2360	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2361	1	EL-CAP	4 M 7	63 V		2222	035 38478	4822	124 40246
2362	1	EL-CAP	4 M 7	63 V		2222	035 38478	4822	124 40246
2363	1	EL-CAP	4 M 7	63 V			035 38478	4822	124 40246
2364	1	CER-CAP	100 N	s 63 V			572 10028	* 5103	109 30600
2365	1	CER-CAP		s 63 V			572 10028	* 5103	109 30600
2366	1	CER-CAP		s 63 V	SIEM.		572 10028		109 30600
2367	1	EL-CAP	4 M 7				035 38478		124 40246
2368	1	CER-CAP	100 N				572 10028		109 30600
2369	1	CER-CAP	100 N	s 63 V	SIEM.	2012	572 10028	* 5103	109 30600
2371	1	CER-CAP	100 N S	63 V	SIEM.	2012	572 10028	* 5103	109 30600
2372	1	CER-CAP		63 V			572 10028		109 30600
2373	1	CER-CAP		63 V			572 10028		109 30600
2374	1	CER-CAP		63 V			572 10028		109 30600
2375	1	CER-CAP		63 V			572 10028		109 30600
2376	1	CER-CAP		63 V			572 10028		109 30600
2377	1	CER-CAP		63 V			572 10028		109 30600
2378	1	CER-CAP		G 100 V			682 28689		109 30530
2379	1	CER-CAP		G 100 V			682 04279		109 30510





SPARE PART CATALOGUE MAINBOARD

ITEM	QTY	DESCRIPTION			CODE NUMBER	SERVICE NUMBER
2381 2382 2383	1 1 1	CER-CAP CER-CAP CER-CAP	270 P G 100 270 P G 100 270 P G 100	v	2222 682 70271 2222 682 70271 2222 682 70271	* 5103 109 30560 * 5103 109 30560 * 5103 109 30560
2390 2391 2392 2393 2394 2395 2396 2397	1 1 1 1 1 1	CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP	100 N S 63 100 N S 63 100 N S 63 100 N S 63 47 P G 100 22 P G 100 100 P G 100 47 P G 100	V SIEM. V SIEM. V SIEM. V V V	2012 572 10028 2012 572 10028 2012 572 10028 2012 572 10028 2222 679 28479 2222 682 10229 2222 682 28101 2222 679 28479	* 5103 109 30600 * 5103 109 30600 * 5103 109 30600 * 5103 109 30600 * 5103 109 30520 * 5103 109 30540 * 5103 109 30520

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SPARE PART CATALOGUE MAINBOARD



ITEM	QTY	DESCRIPTION		CODE	NUMBER	SERVICE NUMBER
4701	1	RES NETWORK	4308R-101-472 BOURNS	2122	118 00117	5322 111 94053
4702	1	RES NETWORK	4116R-003-221/331	2122	118 00238	5322 111 10318
4703	1	RES NETWORK	4308R-101-472 BOURNS	2122	118 00117	5322 111 94053
4704	1	RES NETWORK	4308R-101-472 BOURNS	2122	118 00117	5322 111 94053
4705	1	RES NETWORK	4308R-101-472 BOURNS	2122	118 00117	5322 111 94053
4706	1	RES NETWORK	4308R-101-472 BOURNS	2122	118 00117	5322 111 94053
4707	1	RES NETWORK	4308R-101-472 BOURNS	2122	118 00117	5322 111 94053
4708	1	RES NETWORK	4308R-101-472 BOURNS	2122	118 00117	5322 111 94053
4709	1	RES NETWORK	4308R-101-472 BOURNS	2122	118 00117	5322 111 94053
4710	1	RES NETWORK	898-3-R22	2122	118 00339	5322 111 94266
4712	1	POT	2 K 2 MTP 10	2322	482 20222	5322 101 14008
4713	1	TRIMPOT	4 K 7	2322	482 20472	5322 100 10114
5101	1	COIL ASSY		5103	108 20220	* 5103 109 30900
7301	1	TRANSISTOR	BC 558 B	9331	977 50112	4822 130 44197
7302	1	TRANSISTOR	BC 549 C	9331	977 00112	4822 130 44246
7303	1	TRANSISTOR	BC 549 C	9331	977 00112	4822 130 44246



SPARE PART CATALOGUE MAINBOARD

ITEM	QTY	DESCRIPTION			CODE	NUMBER	SERVICE NUMBER
3301	1	RESISTOR (AMMOPACK)	220 R	J CR25	2322 211	73221	4822 110 73089
3302	ĩ	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73089
3303	1	RESISTOR (AMMOPACK)	10 K	J CR25	2322 211		4822 110 73134
3304	î	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73134
3305	1	RESISTOR (AMMOPACK)	4 K 7	J CR25	2322 211		4822 110 73125
3306	i	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73125
3307	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73125
3308	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73107
3309	1	RESISTOR (AMMOPACK)	12 K	J CR25	2322 211		4822 110 73136
3309	1	RESISTOR (APPROPAGE)	12 K	J CRZJ			
3310	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73127
3311	1	RESISTOR (AMMOPACK)	4 K 7	J CR25	2322 211		4822 110 73125
3313	1	MET-RES-LAC	2 K67	F MR25	2322 151		5322 116 54578
3314	1	RESISTOR (AMMOPACK)	680 R	J CR25	2322 211		4822 110 73103
3315	1	RESISTOR (AMMOPACK)	1 K	J CR25	2322 211		4822 110 73107
3316	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73116
3317	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73116
3318	1	RESISTOR (AMMOPACK)	2 K 2	J CR25	2322 211	. 73222	4822 110 73116
3319	1	MET-RES-LAC	2 K67	F MR25	2322 151	. 52672	5322 116 54578
3320	1	MET-RES-LAC	3 K48	F MR25	2322 151		5322 116 55367
3321	1	MET-RES-LAC	3 K48	F MR25	2322 151		5322 116 55367
3322	1	MET-RES-LAC	1 K10	F MR25	2322 151		4822 116 51236
3323	1	RESISTOR	10 K	F MR25	2322 151		4822 110 73134
3324	1	MET-RES-LAC	1 K10	F MR25	2322 151		4822 116 51236
3325	1	RESISTOR	10 K	F MR25	2322 151		4822 110 73134
3326	1	MET-RES-LAC	1 K21	F MR25	2322 151	51212	5322 116 54557
3327	1	MET-RES-LAC	1 K	F MR25	2322 151	51002	4822 116 51235
3328	1	CARB-RES	160 R	J MR25	2322 212	13161	4822 110 51931
3329	1	RESISTOR (AMMOPACK)	470 R	J CR25	2322 211	73471	4822 110 73098
3330	1	RESISTOR (AMMOPACK)	4 K 7	J CR25	2322 211		4822 110 73125
3331	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73083
3332	1	RESISTOR (AMMOPACK)	4 K 7	J CR25	2322 211		4822 110 73125
3333	1	RESISTOR (AMMOPACK)	10 K	J CR25	2322 211		4822 110 73134
3334	1	RESISTOR (AMMOPACK)	22 R	J CR25	2322 211		4822 110 73063
3335	1	RESISTOR (AMMOPACK)	22 R	J CR25	2322 211	73229	4822 110 73063
3336	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73094
3337	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73089
3338	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73083
3339	1	RESISTOR (AMMOPACK)	270 R	J CR25	2322 211	73271	4822 110 73092
3340	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73096
3341	1	RESISTOR (AMMOPACK)	27 K	J CR25	2322 211		4822 110 73145
3342	1	RESISTOR (AMMOPACK)	18 K	J CR25	2322 211		4822 110 73141
3343	1	RESISTOR (AMMOPACK)		J CR25	2322 211		4822 110 73087
3344	1	RESISTOR (AMMOPACK)	10 K	J CR25	2322 211		4822 110 73134
3345	1	RESISTOR (AMMOPACK)	4 K 7	J CR25	2322 211		4822 110 73125
3346	1	RESISTOR (AMMOPACK)	1 K	J CR25	2322 211	73102	4822 110 73107

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SPARE PART CATALOGUE MAINBOARD



ITEM	QTY			CODE	NUMBER	SERVICE NUMBER
7401	1	I.C. MC 1489		0332	912 00112	5322 209 84308
7402	ī	I.C. MC 1488		9332	963 20112	5322 209 84307
7403	1	I.C. MC 1489		9332	912 00112	5322 209 84308
7405	1	I.C. MC 1488		9332	963 20112	5322 209 84307
7407	1	I.C. 74 LS 08 A		9332	869 50112	5322 209 84995
7408	1	I.C. 74 LS 32 A		9332	870 90112	5322 209 85311
7409	1	I.C. 74 LS 38 A		9332	871 10112	5322 209 85605
7410	1	I.C. 74 LS 240 N	(TI)	9334	182 20682	5322 209 85862
7411	1	I.C. 74 S 38 N			920 50112	5322 209 85677
7412	1	I.C. 74 LS 240 N	(TI)		182 20682	5322 209 85862
7413	1.	I.C. 74 S 38 N			920 50112	5322 209 85677
7414	1	I.C. 74 LS 00 A			869 00112	5322 209 84823
7415	1	I.C. 74 LS 221 B			875 70112	* 5103 109 31020
7416	1	I.C. 74 S 112 N			877 80112	5322 209 85741
7417	1	I.C. MC 4024 P			201 50682	5322 209 85819
7418	1	I.C. 74 LS 244		9334	307 60112 700 70112	5322 209 86017
7419	1	I.C. 74 LS 125		9333	700 70112	5322 209 85966
7420	1	I.C. 74 LS 125		9333	700 70112	5322 209 85966
7421	1	I.C. P 8251 A	(INTEL)	9334	665 60682	5322 209 85847
7422	1	I.C. 74 LS 74 AN			617 20112	4822 209 80782
7423	1	I.C. 74 LS 08 A		9332	869 50112	5322 209 84995
7424	1	I.C. 74 LS 08 A			869 50112	5322 209 84995
7425	1	I.C. 74 LS 08 A			869 50112	5322 209 84995
7426	1	I.C. 74 LS 32 A			870 90112	5322 209 85311
7427	1	I.C. 74 LS 32 A			870 90112	
7428	1	I.C. 74 LS .08 A			869 50112	
7429	1	I.C. 74 LS 74 AN		9334	617 20112	4822 209 80782
7430	1	I.C. 74 LS 156 N			121 50112	4822 209 80446
7431	1	I.C. 74 LS 367 N			043 40112	5322 209 85558
7432	1 .	I.C. 74 LS 373 N			555 00112	5322 209 86062
7433	1	I.C. 74 LS 293 A			876 60112	5322 209 86016
7434	1	I.C. 74 LS 14 N			870 10112	5322 209 85199
7435	1	I.C. 74 LS 244			307 60112	5322 209 86017
7436	1	I.C. 74 LS 244	(0.77.00)		307 60112	5322 209 86017
7437	1		(ZILOG)		977 60682	
7438 7439	1 1	I.C. 74 LS 373 N I.C. 74 LS 245	(TI)		555 00112 628 70682	
7440	1	I.C. P 8257-5		933/	671 30682	5322 209 86551
7441	i	I.C. Z80 A - SIO - 0			949 30682	* 5103 109 31200
7442	1	I.C. 74 S 157 N			878 90112	5322 209 85669
7443	1	I.C. 74 LS 107			872 80112	5322 209 85816
7444	1	I.C. 74 LS 04 A			869 30112	4822 209 80783
7445	ī	I.C. 74 LS 10 A			869 70112	5322 209 84996
7446	1	I.C. 74 LS 74 AN			617 20112	4822 209 80782
7447	1	I.C. 74 LS 74 AN			617 20112	4822 209 80782
7448	1	I.C. 74 S 08 N			876 90112	5322 209 85681
7449	1	I.C. Z80 A - CTC	(ZILOG)		977 50682	5322 209 14717





SPARE PART CATALOGUE MAINBOARD

ITEM	QTY	DESCRIPTION	CODE NUMB	ER SERVICE NUMBER
	_		0225 077 506	82 5322 209 14717
7450	1	I.C. Z80 A - CTC (ZILOG)	9335 977 506	
7451	1	I.C. PD 765	9335 284 706	
7452	1	I.C. 74 LS 04 A	9332 869 301	
7453	1	I.C. 74 LS 38 A	9332 871 101	
7554	1	I.C. 74 LS 244	9334 307 601	
7455	1	I.C. 74 LS 38 A	9332 871 101	
7456	1	ROM $4K \times 8$ (7456)	5103 108 735	
7457	1	I.C. 74 S 32 N	9332 877 201	
7458	1	I.C. 74 LS 14 N	9332 870 101	
7459	1	I.C. 74 LS 14 N	9332 870 101	12 3322 209 63199
7460	1	I.C. 74 LS 00 A	9332 869 001	
7461	1	I.C. 74 LS 74 AN	9332 617 201	
7462	1	I.C. 82 S 129 N PROG. (7462)	5103 108 523	
7463	1	I.C. 74 LS 32 A	9332 870 901	
7464	1	I.C. 74 S 00 N	9332 813 801	
7465	1	I.C. 74 LS 00 A	9332 869 001	
7466	1	I.C. 74 S 32 N	9332 877 201	
7467	1	I.C. 74 LS 04 A	9332 869 301	
7468	1	I.C. 74 LS 175 N	9332 874 901	12 5322 209 84999
7471	1	I.C. 705 MIN 7406 A	9332 830 601	12 5322 209 86327
7472	1	I.C. 74 S 157 N	9332 878 901	12 5322 209 85669
7473	ī	I.C. 74 S 157 N	9332 878 901	12 5322 209 85669
7474	1	I.C. 74 LS 139 N	9332 873 601	12 5322 209 85839
7475	ī	I.C. 74 LS 138 B	9332 873 501	12 5322 209 85647
7476	1	I.C. 74 LS 139 N	9332 873 601	12 5332 209 85839
7478	1	I.C. HM 4864-2 (HITJ)	9336 043 106	82 5322 209 80977
7479	1	I.C. HM 4864-2 (HITJ)	9336 043 106	5322 209 80977
7480	1	I.C. HM 4864-2 (HITJ)	9336 043 106	582 5322 209 80977
7481	1	I.C. HM 4864-2 (HITJ)	9336 043 106	
7482	1	I.C. HM 4864-2 (HITJ)	9336 043 106	
7483	1	I.C. HM 4864-2 (HITJ)	9336 043 106	
7484	1	I.C. HM 4864-2 (HITJ)	9336 043 106	
7485	ī	I.C. HM 4864-2 (HITJ)	9336 043 106	
7486	ī	I.C. 74 LS 74 AN	9332 617 201	
7487	1	I.C. 74 S 38 N	9332 920 501	
7488	1	I.C. 74 LS 74 AN	9334 617 201	
7489	ī	I.C. 74 LS 669 (TI)	9335 970 406	
7490	1	I.C. 74 LS 669 (TI)	9335 970 406	582 5322 209 81026
7491	1	I.C. uA 741 CN	9332 404 201	
7501	1	DIODE 1N4148	9330 839 901	4822 130 30621
7502	1	DIODE 1N4148	9330 839 901	
7503	î	DIODE BZX 79/C5V6	9331 177 301	
7504	1	DIODE 1N4148	9330 839 903	•
7505	1	DIODE BZX 79/C5V6	9331 177 30	
7505 7506	1	DIODE OA 91	9330 000 803	
7507	1	DIODE OA 91	9330 000 803	
1 301	1	DIODE ON 71	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
7601	1	QUARTZ 16 MHz	8203 235 108	340 * 5103 109 30950

SPARE PART CATALOGUE MAINBOARD



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SPARE PART CATALOGUE TERMINALBOARD

ITEM	QTY	DESCRIPTION		CODE NUMBER	SERVICE NUMBER
64	1	TERMINALBOARD PCB ASSY		5103 108 02720	* 5103 109 30010
2 3 4 5 9	1 1 1 1	SOCKET 4-pin 0-826375-4 SOCKET 6-pin 0-826375-6 SOCKET 7-pin 0-826375-7 SOCKET 8-pin 0-826375-8 SOCKET 5-pin	(AMP) (AMP) (AMP) (AMP)	2422 025 04092 2422 038 00122 2422 038 00123 2422 025 04093 3103 308 70060	* 5103 109 30400 * 5103 109 30400 * 5103 109 30400 * 5103 109 30400 4822 267 50218
10 11 12 20	1 1 1	IC-SOCKET 40-pin IC-SOCKET 28-pin IC-SOCKET 24-pin SOCKET 4-pin 0-826372-4	(AMP)	3103 238 73270 3103 238 73260 3103 238 73250 2422 038 00125	5322 255 44217 5322 255 44047 5322 255 44171 * 5103 109 30400
2305 2306 2307 2308 2312 2313 2314 2315 2317 2318	1 1 1 1 1 1 1 1	CER-CAP 100 N S CER-CAP 100 N S EL-CAP 4 M 7 CER-CAP 100 N S CER-CAP 100 N S CER-CAP 100 N S EL-CAP 4 M 7	63 V SIEM.	2012 572 10028 2012 572 10028 2012 572 10028 2012 572 10028 2012 572 10028 2222 035 38478 2012 572 10028 2012 572 10028 2012 572 10028 2012 572 10028 2012 572 10028	* 5103 109 30600 * 5103 109 30600 * 5103 109 30600 * 5103 109 30600 * 5103 109 30600 4822 124 40246 * 5103 109 30600 * 5103 109 30600 * 5103 109 30600 4822 124 40246 * 5103 109 30600
2319 2320 2321 2322 2323 2324 2325 2326 2327 2328 2329	1 1 1 1 1 1 1 1	CER-CAP 100 N S CER-CAP 4 M 7 CER-CAP 100 N S CER-CAP 100 N S CER-CAP 100 N S CER-CAP 100 N S CER-CAP 100 N S	63 V SIEM	2012 572 10028 2012 572 10028 2022 035 38478 2012 572 10028 2012 572 10028 2012 572 10028 2012 572 10028	* 5103 109 30600 * 5103 109 30600 4822 124 40246 * 5103 109 30600 * 5103 109 30600
2330 2331 2332 2333 2334 2335 2336 2337 2338 2339	1 1 1 1 1 1 1 1	CER-CAP 100 N S CER-CAP 100 N S CER-CAP 100 N S CER-CAP 100 N S EL-CAP 4 M 7 CER-CAP 100 N S CER-CAP 100 N S	63 V SIEM 63 V SIEM 63 V SIEM 63 V SIEM 63 V SIEM 63 V SIEM 63 V SIEM	• 2012 572 10028 • 2012 572 10028	* 5103 109 30600 * 5103 109 30600 * 5103 109 30600 4822 124 40246 * 5103 109 30600 * 5103 109 30600 * 5103 109 30600 * 5103 109 30600

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SPARE PART CATALOGUE TERMINALBOARD



ITEM	QTY	DESCRIPTION			CODE	NUMBER	SERVICE NUMBER
2340	1	CER-CAP	100 N S	63 V SIEM	. 2012 57	72 10028	5103 109 30600
2341	1	CER-CAP	100 N S	63 V SIEM	. 2012 57	72 10028 3	5103 109 30600
2342	1	CER-CAP	100 N S	63 V SIEM	. 2012 57		5103 109 30600
2343	1	CER-CAP	100 N S	63 V SIEM	. 2012 57		5103 109 30600
2344	1	CER-CAP	100 N S	63 V SIEM			5103 109 30600
2345	1	CER-CAP	100 N S	63 V SIEM	. 2012 57		5103 109 30600
2346	1	CER-CAP	100 N S	63 V SIEM			5103 109 30600
2347	1	CER-CAP	100 N S	63 V SIEM	. 2012 57		5103 109 30600
2348	1	CER-CAP	100 N S		. 2012 57		5103 109 30600
2349	1	CER-CAP	100 N S		. 2012 57		5103 109 30600
2350	1	CER-CAP	100 N S		. 2012 57		5103 109 30600
2351	1	EL-CAP	4 M 7	63 V	2222 03	35 38478	4822 124 40246
2352	1	CER-CAP	100 N S		 2012 57 		5103 109 30600
2353	1	CER-CAP	100 N S	63 V SIEM	 2012 57 	72 10028 ×	5103 109 30600
2354	1	CER-CAP	100 N S	63 V SIEM	2012 57	72 10028 *	5103 109 30600
2355	1	CER-CAP	100 N S		2012 57	72 10028 🔻	5103 109 30600
2356	1	CER-CAP	100 N S		2012 57		5103 109 30600
2357	1	CER-CAP	100 N S	63 V SIEM	. 2012 57	72 10028 *	5103 109 30600
2358	1	CER-CAP	100 N S	63 V SIEM	2012 57	⁷ 2 10028 *	5103 109 30600
2359	1	CER-CAP	100 N S	63 V SIEM	• 2012 57	⁷ 2 10028 *	5103 109 30600
2360	1	CER-CAP	100 N S	63 V SIEM	. 2012 57	′2 10028 *	5103 109 30600
2361	1	CER-CAP	100 N S	63 V SIEM	2012 57	⁷ 2 10028 *	5103 109 30600
2362	1	CER-CAP	100 N S	63 V SIEM	. 2012 57	⁷ 2 10028 *	5103 109 30600
2363	1	CER-CAP	100 N S	63 V SIEM	2012 57	['] 2 10028 *	5103 109 30600
2364	1	CER-CAP	100 N S	63 V SIEM	2012 57		5103 109 30600
2365	1	CER-CAP	100 N S	63 V SIEM	. 2012 57		5103 109 30600
2366	1	CER-CAP	100 N S		2012 57		5103 109 30600
2367	1	CER-CAP	100 N S		2012 57		5103 109 30600
2368	1	CER-CAP	100 N S		2012 57		5103 109 30600
2369	1	CER-CAP	100 N S		2012 57		5103 109 30600
2370	1	EL-CAP	4 M 7	63 V	2222 03	35 38478	4822 124 40246
2371	1	CER-CAP	100 N S	63 V SIEM	2012 57	['] 2 10028 *	5103 109 30600
2372	1	CER-CAP	100 N S	63 V SIEM	2012 57	['] 2 10028 *	5103 109 30600
2373	1	CER-CAP	100 N S	63 V SIEM	. 2012 57	['] 2 10028 *	5103 109 30600
2374	1	CER-CAP	100 N S	63 V SIEM	2012 57	'2 10028 *	5103 109 30600
2375	1	CER-CAP	100 N S	63 V SIEM	2012 57	'2 10028 *	5103 109 30600
2376	1	CER-CAP	100 N S		2012 57		5103 109 30600
2377	1	EL-CAP	4 M 7	63 V	2222 03	35 38478	4822 124 40246
2378	1	CER-CAP	100 N S	63 V SIEM	2012 57	2 10028 *	5103 109 30600
2379	1	CER-CAP	100 N S	63 V SIEM	2012 57	2 10028 *	5103 109 30600
2380	1	EL-CAP	4 M 7	63 V		5 38478	4822 124 40246
2381	1	CER-CAP	100 N S	63 V SIEM	2012 57		5103 109 30600
2382	1	CER-CAP	100 N S	63 V SIEM	2012 57	2 10028 *	5103 109 30600
2383	1	CER-CAP	100 N S	63 V SIEM	2012 57	2 10028 *	5103 109 30600
2384	1	CER-CAP	100 N S	63 V SIEM	2012 57	2 10028 *	5103 109 30600
2385	1	CER-CAP	100 N S	63 V SIEM	2012 57	2 10028 *	5103 109 30600
2386	1	CER-CAP	100 N S		2012 57		5103 109 30600
2387	1	CER-CAP	100 N S		2012 57		5103 109 30600
2388	1	CER-CAP	100 N S		2012 57	2 10028 *	5103 109 30600
2389	1	CER-CAP	100 N S	63 V SIEM.	2012 57		5103 109 30600





SPARE PART CATALOGUE TERMINALBOARD

ITEM	QTY	DESCRIPTION		CODE	NUMBER	SERVICE NUMBER
	·			0000	025 20470	4822 124 40246
2390	1	EL-CAP	4 M 7 63 V		035 38478	
2391	1	CER-CAP	120 P G 100 V		682 70121	* 5103 109 30550 * 5103 100 30570
2392	1	CER-CAP	390 P G 100 V		682 70391	* 5103 109 30570
2393	1	CER-CAP	100 N 63 V		572 10011	5322 122 34238
2394	1	EL-CAP	4 M 7 63 V		035 38478	4822 124 40246
2395	1	CER-CAP	200		572 10028	* 5103 109 30600
2396	1	CER-CAP	100 11 0 00 1 41		572 10028	* 5103 109 30600
2397	1	CER-CAP			572 10028	* 5103 109 30600
2398	1	CER-CAP	100 11 5 00		572 10028	* 5103 109 30600
2399	1	CER-CAP	100 N S 63 V SI	EM. 2012	572 10028	* 5103 109 30600
						# 5100 100 20C00
2400	1	CER-CAP	100 11 0 00		572 10028	* 5103 109 30600
2401	1	EL-CAP	4 M 7 63 V		035 38478	4822 124 40246
2402	1	CER-CAP	200 11 0 00 1 ==		572 10028	* 5103 109 30600
2403	1	EL-CAP	33 M 16 V		035 35339	4822 124 40272
2404	1	EL-CAP	4 M 7 63 V		035 38478	4822 124 40246
2405	1	EL-CAP	4 M 7 63 V		035 38478	4822 124 40246
2406	1	EL-CAP	4 M 7 63 V		035 38478	4822 124 40246
2407	1	EL-CAP	33 M 16 V		035 35339	4822 124 40272
2408	1	CER-CAP	68 P G 100 V		682 28689	* 5103 109 30530
2409	1	CER-CAP	27 P G 100 V	2222	682 04279	* 5103 109 30510
						+ F100 100 00F00
2410	1	CER-CAP	68 P G 100 V		682 28689	* 5103 109 30530
2411	1	CER-CAP	200 1, 2 00 ,		572 10028	* 5103 109 30600
2412	1	CER-CAP	200 21 2 00 1		572 10028	* 5103 109 30600
2413	1	EL-CAP	4 M 7 63 V		035 38478	4822 124 40246
2414	1	CER-CAP	100 11 0 00 1 1 1		572 10028	* 5103 109 30600
2415	1	CER-CAP			572 10028	* 5103 109 30600
2416	1	CER-CAP			572 10028	* 5103 109 30600
2417	1	CER-CAP			572 10028	* 5103 109 30600
2418	1	CER-CAP			572 10028	* 5103 109 30600
2419	1	CER-CAP			572 10028	* 5103 109 30600
2420	1	CER-CAP	100 N S 63 V SI	EM. 2012	572 10028	* 5103 109 30600

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SPARE PART CATALOGUE TERMINALBOARD



ITEM	QTY	DESCRIPTION	CODE NUMBER	SERVICE NUMBER
3301	1	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
3302	1	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
3303	1	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
3304	1	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
3305	1	RESISTOR (AMMOPACK) 100 R J CR25	2322 211 73101	4822 110 73081
3306	1	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
3307	ī	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
3308	1	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
3309	1	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
		, , , , ,	, , , , ,	1022 110 75110
3310	1	RESISTOR (AMMOPACK) 10 R J CR25	2322 211 73109	4822 110 73054
3311	1	RESISTOR (AMMOPACK) 10 R J CR25	2322 211 73109	4822 110 73054
3312	1	RESISTOR (AMMOPACK) 10 R J CR25	2322 211 73109	4822 110 73054
3313	1	RESISTOR (AMMOPACK) 10 R J CR25	2322 211 73109	4822 110 73054
3314	1	RESISTOR (AMMOPACK) 100 R J CR25	2322 211 73101	4822 110 73081
3315	1	RESISTOR (AMMOPACK) 100 R J CR25	2322 211 73101	4822 110 73081
3316	1	RESISTOR (AMMOPACK) 4 K 7 J CR25	2322 211 73472	4822 110 73118
3317	1	RESISTOR (AMMOPACK) 100 R J CR25	2322 211 73101	4822 110 73081
3318	1	RESISTOR (AMMOPACK) 390 R J CR25	2322 211 73391	4822 110 73096
3319	1	RESISTOR (AMMOPACK) 100 R J CR25	2322 211 73101	4822 110 73081
		,		
3320	1	RESISTOR (AMMOPACK) 470 R J CR25	2322 211 73471	4822 110 73098
3321	1	RESISTOR (AMMOPACK) 330 R J CR25	2322 211 73331	4822 110 73094
3322	1	RESISTOR (AMMOPACK) 330 R J CR25	2322 211 73331	4822 110 73094
3323	1	RESISTOR (AMMOPACK) 270 R J CR25	2322 211 73271	4822 110 73092
3324	1	RESISTOR (AMMOPACK) 220 R J CR25	2322 211 73221	4822 110 73089
3325	1	RESISTOR (AMMOPACK) 100 R J CR25	2322 211 73101	4822 110 73081
3326	1	RESISTOR (AMMOPACK) 150 R J CR25	2322 211 73151	4822 110 73085
3327	1	RESISTOR (AMMOPACK) 100 R J CR25	2322 211 73101	4822 110 73081
3328	1	RESISTOR (AMMOPACK) 180 R J CR25	2322 211 73181	4822 110 73087
3329	1	RESISTOR (AMMOPACK) 330 R J CR25	2322 211 73331	4822 110 73094
	_			
3330	1	RESISTOR (AMMOPACK) 330 R J CR25	2322 211 73331	4822 110 73094
3331	1	RESISTOR (AMMOPACK) 330 R J CR25	2322 211 73331	4822 110 73094
3332	1	RESISTOR (AMMOPACK) 10 K J CR25	2322 211 73103	4822 110 73134
3333	1	RESISTOR (AMMOPACK) 1 K 2 J CR25	2322 211 73122	4822 110 73109
3334	1	RESISTOR (AMMOPACK) 18 K J CR25	2322 211 73183	4822 110 73141
3335	1	RESISTOR (AMMOPACK) 390 R J CR25	2322 211 73391	4822 110 73096
3336	1	RESISTOR (AMMOPACK) 27 K J CR25		4822 110 73145
3337		RESISTOR (AMMOPACK) 180 R J CR25		
3338	1			
3339	1	RESISTOR (AMMOPACK) 100 R J CR25	2322 211 73101	4822 110 73081
3340	1	RESISTOR (AMMOPACK) 100 K J CR25	9999 911 7910/	6000 110 70161
3340	1	RESISION (AMMOPACK) 100 K J CR25	2322 211 /3104	4822 110 /3161
4301	1	RES NETWORK 898-3-R22	2122 118 00339	5322 111 94266
4302	1	RES NETWORK 898-3-R22	2122 118 00339	
4303	1	RES NETWORK 4310R-101-472 BOURNS	3103 200 57740 *	5103 109 30830
4304	1	RES NETWORK 4310R-101-472 BOURNS	3103 200 57740 *	5103 109 30830
4305	1	RES NETWORK 4310R-101-472 BOURNS RES NETWORK 4310R-101-472 BOURNS	3103 200 57740 *	5103 109 30830
	_			
5301			5103 108 20270 *	
5302	1	CHOKE 552-5373-14-02-00 1MU2	8203 235 19650 *	5103 109 30920





SPARE PART CATALOGUE TERMINALBOARD

ITEM	QTY	DESCR	IPTION		CODE	N	IUMBER		SERVI	CE 1	NUMBER
7404	1	I.C.	74 LS 74 AN	(INTEL) (ZILOG)	9334	617	20112		4822	209	80782
7405	ĩ	I.C.	74 LS 290 A		9332		50112				86015
7406	î	I.C.	P 8251 A	(INTEL)	9334		60682				85847
7407	1	I.C.	Z80A CTC	(ZILOG)	9335	977	50682				14717
7408	i	I.C.	Z80A CPII	(ZILOG)	9335	977	60682				10179
7409	ī	ROM	8K x 8 - 2664	(ZILOG) (ZILOG) (7409)	5103	108	73570	*			31120
7407	1	ROH	OR A 0 2004	(740))	3103	100	. 33, 0		3103		J1-40
7410	1	I.C.	74 S 139 N		9332	878	50112				85673
7411	1	I.C.	74 LS 32 A		9332	870	90112				85311
7412	1	I.C.	MC 68450	(MTLA)	9335	354	40682		5322	209	10176
7413	1	I.C.	74 LS 257 AN		9334	670	10112		5322	209	86334
7414	1	I.C.	74 LS 197 N		9332	919	50112		5322	209	85612
7415	1	I.C.	74 LS 197 N		9332	919	50112		5322	209	85612
7416	1	I.C.	74 LS 257 AN		9334	670	10112		5322	209	86334
7417	1	I.C.	74 LS 257 AN		9334	670	10112				86334
7418	1	I.C.	74 LS 257 AN		9334	670	10112				86334
7419	ī	I.C.	74 LS 257 AN		9334	670	10112 10112 10112				86334
7420	1	I.C.	74 LS 197 N				50112				85612
7421	1	I.C.	74 LS 197 N				50112				85612
7422	1	I.C.	74 LS 257 AN				10112				86334
7423	1	I.C.	74 LS 257 AN				10112				86334
7424	1	I.C.	74 LS 257 AN				10112				86334
7425	1	I.C.	416 C-5 NEC				80682				50108
7426	1	I.C.	416 C-5 NEC				80682				50108
7427	1	I.C.	416 C-5 NEC				80682				50108
7428	1	I.C.	416 C-5 NEC				80682				50108
7429	1	I.C.	416 C-5 NEC		9336	549	80682		5322	209	50108
7430	1	I.C.	416 C-5 NEC		9336	549	80682		5322	209	50108
7431	1	I.C.	416 C-5 NEC		9336	549	80682		5322	209	50108
7432	1	I.C.	416 C-5 NEC		9336	549	80682		5322	209	50108
7433	1	I.C.	416 C-5 NEC				80682				50108
7434	1	I.C.	416 C-5 NEC				80682				50108
7435	1	I.C.	416 C-5 NEC				80682				50108
7436	1	I.C.	416 C-5 NEC				80682				50108
7437	1	I.C.	416 C-5 NEC				80682				50108
7438	1	I.C.					80682				50108
7439	1	I.C.	416 C-5 NEC		9336	549	80682		5322	209	50108
7440	1	I.C.	416 C-5 NEC		9336	549	80682		5322	209	50108
7441	1	I.C.	74 LS 244		9334	307	80682 60112		5322	209	86017
7442	1	I.C.	74 LS 273		9334	121	80112		5322	200	85792
7443	1	I.C.	74 S 373 N				00112	*			31010
7444	ī	I.C.	74 LS 244				60112	••			86017
7445	1	I.C.	74 LS 244	(TI)			70682				86225
7446	1	I.C.	74 LS 244	\/			60112				86017
7447	1	I.C.	74 LS 244 74 LS 373 N				00112				86062
7448	1	I.C.	74 LS 373 N						5322	200	95600
7449	1		74 LS 155 N		3102	200	90112 57320		5222	200	02400
7447	T	I.C.	14 F2 T00		2103	200	57320		3322	209	86292

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SPARE PART CATALOGUE TERMINALBOARD



ITEM	QTY	DESCRIPTION	CODE	NUMBER	SERVICE NUMBER
7450	1	ROM $4K \times 8 - 2632$ (7450)	5103	108 73580	* 5103 109 31130
7451	1	I.C. 74 LS 273	9334	121 80112	5322 209 85792
7452	1	I.C. 74 LS 273	9334	121 80112	5322 209 85792
7453	1	I.C. 74 LS 273	9334	121 80112	5322 209 85792
7454	1	I.C. 74 LS 273	9334	121 80112	5322 209 85792
7455	1	I.C. 74 LS 195 AN	9333	176 80112	5322 209 85939
7456	1	I.C. 74 LS 195 AN	9333	176 80112	5322 209 85939
7457	1	I.C. 74 LS 74 AN	9334	617 20112	4822 209 80782
7458	1	I.C. 74 S 169 N-00 (TI)	9334	995 70682	* 5103 109 31000
7459	1	ROM 4K x 8 - 2632 (7450) I.C. 74 LS 273 I.C. 74 LS 273 I.C. 74 LS 273 I.C. 74 LS 273 I.C. 74 LS 195 AN I.C. 74 LS 195 AN I.C. 74 LS 74 AN I.C. 74 S 169 N-00 (TI) I.C. 74 S 04 N	9332	617 40112	5322 209 84475
7460	1	I.C. 74 S 04 N	9332	617 40112	5322 209 84475
7461	1	I.C. 74 LS 32 A	9332	870 90112	5322 209 85311
7462	1	I.C. 74 LS 32 A	9332	870 90112	5322 209 85311
7463	1	I.C. 74 LS 74 AN	9334	617 20112	4822 209 80782
7464	1	I.C. 74 LS 74 AN	9334	617 20112	4822 209 80782
7465	1	I.C. 74 S 32 N	9332	877 20112	5322 209 85679
7466	1	I.C. 74 LS 04 A	9332	869 30112	4822 209 80783
7.467	1	I.C. 74 LS 32 A	9332	870 90112	5322 209 85311
7468	1	I.C. 74 LS 293 A	9332	876 60112	5322 209 86016
7469	1	I.C. 7407 A	9332	830 80112	5322 209 84761
7470	1	I.C. 7407 A	9332	830 80112	5322 209 84761
7471	1	I.C. 74 LS 10 A	9332	869 70112	5322 209 84996
7472	1	I.C. 74 LS 02 N	9332	876 80112	5322 209 85407
7473	1	I.C. 74 S 00 N	9332	813 80112	5322 209 84167
7474	1	I.C. 74 LS 00 A	9332	869 00112	5322 209 84823
7475	1	I.C. 74 LS 86 A	9332	872 20112	5322 209 84997
7476	1	I.C. 74 LS 399 N-00 (TI)	9335	105 70682	* 5103 109 31030
7477	1	I.C. 74 LS 157 B	9332	874 00112	5322 209 85489
7478	1	I.C. 74 LS 10 A	9332	869 70112	5322 209 84996
7479	1	I.C. 74 LS 14 N	9332	870 10112	5322 209 84475 5322 209 85311 5322 209 85311 4822 209 80782 4822 209 80782 5322 209 85679 4822 209 80783 5322 209 85679 4822 209 86016 5322 209 84761 5322 209 84761 5322 209 8496 5322 209 84823 5322 209 84823 5322 209 84823 5322 209 84897 * 5103 109 31030 5322 209 85489 5322 209 85489 5322 209 85499
7480	1	I.C. 74 S 08 N	9332	876 90112	5322 209 85681
7501	1	DIODE OA 91 DIODE BZX 79/C5V1	9330	000 80113	4822 130 30191
7502	- 1	DIODE BZX 79/C5V1	9331	177 20113	4822 130 34233
7601	1	TRANSISTOR BC 558 B	9331	977 50112	5322 130 44197
7602	1	QUARTZ 12.288 MHz	8203	235 19240	* 5103 109 30960
7603	. 1	TRANSISTOR BC 558 B QUARTZ 12.288 MHz CER. RESONATOR	5103	108 70670	5322 280 14028





SPARE PART CATALOGUE KEYBOARD

ITEM	QTY	DESCRIPTION	CODE NUMBER	SERVICE NUMBER
	1	KEYBOARD PCB-ASSY	5103 108 02760	* 5103 109 30030
2	1	SWITCH LP ASSY (92 OFF)	5112 291 43290	* 5103 109 30340
3	1	SWITCH LE ASSY (2 OFF)	5112 291 42910	* 5103 109 30350
13	1	SOCKET 6-pin	2422 026 00264	* 5103 109 30330
2101	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2102	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2103	1	CER-CAP CL. 1 100 P G 100 V	2222 682 28101	* 5103 109 3 0540
2104	ī	CER-CAP CL.1 100 P G 100 V	2222 682 28101	* 5103 109 30540
2101	1	RESISTOR (AMMOPACK) 2 K 2 J CR25	2322 211 73222	4822 110 73116
3101		RESISTOR (AMMOPACK) 2 K 2 J CR25	2322 211 73222	
3102	1	RESISTOR (AMMOPACK) 270 R J CR25	2322 211 73271	
3103	1	RESISTOR (AMMOPACK) 1 K J CR25		
3104	1	DEGLETOD (AMMODACK) 1 K J CR2J		
3105	1	RESISTOR (AMMOPACK) 2 K 2 J CR25 RESISTOR (AMMOPACK) 2 K 2 J CR25	2322 211 73222	
3106	1	RESISTOR (AMMOPACK) 2 K 2 J CR25	2322 211 /3222	4022 110 /3110
4101	1	RES NETWORK 4310R-101-222	2122 118 00326	* 5103 109 30820
7001	1	L.E.D. LD 30/1	9333 203 30112	* 5103 109 31300
7101	1	I.C. 74 LS 74 AN I.C. 74 LS 10 A I.C. 74 150 N	9334 617 20112	
7102	1	I.C. 74 LS 10 A	9332 869 70112	
7103	1	I.C. 74 150 N	9332 564 30112	* 5103 109 31050
7104	1	I.C. 74 LS 290 A	9332 876 50112	5322 209 86015
7105	1	I.C. 74 LS 293 A	9332 876 60112	5322 209 86016
7106	1	I.C. 74 150 N I.C. 74 LS 290 A I.C. 74 LS 293 A I.C. 74 159 N-00 (TI)	9335 010 40682	* 5103 109 31040
7150	1	VOLTAGE REG. 7805 CU	9332 996 00112	* 5103 109 31310
1	1	KEYBOARD CASE KEYBOARD MASK RUBBER FOOT	5103 104 18770	
8	1	KEYBOARD MASK	5103 104 18760	
9	4	RUBBER FOOT	5103 104 40940	* 5103 109 30240

SPARE PART CATALOGUE KEYBOARD



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SPARE PART CATALOGUE IEEE-BOARD

ITEM	QTY	DESCRIPTION			CODE	NUMBER	SERVICE NUMBER
95	1	IEEE-BOARD (IEC-BUS) PC	B ASSY		5103 108	3 02900 *	5103 109 30040
2	1	SOCKET 24-pin			2422 025	04295	5103 109 30380
2101	1	CER-CAP 100 N S	63 V S	SIEM.	2012 572		* 5103 109 30600
2102	1	CER-CAP 100 N S		SIEM.	2012 572		5103 109 30600
2103	1	EL-CAP 4 M7	63 V		2222 035		4822 124 40246
2104	1	CER-CAP 100 N S			2012 572		* 5103 109 30600
2105	1	CER-CAP 100 N S			2012 573		* 5103 109 30600
2106	1	CER-CAP 100 N S			2012 57		* 5103 109 30600
2107	1	CER-CAP 100 N S			2012 57		* 5103 109 30600
2108	1	CER-CAP 100 N S	-		2012 57		* 5103 109 30600
2109	1	CER-CAP 100 N S			2012 57		* 5103 109 30600
2110	1	CER-CAP 100 N S	63 V S	SIEM.	2012 57	2 10028 3	* 5103 109 30600
3101	1	RESISTOR (AMMOPACK) 6	5 К 2 Ј (CR25	2322 21	1 73622	4822 110 70128
3102	ī			CR25	2322 21	1 73622	4822 110 70128
3103	1			CR25	2322 21	1 73622	4822 110 70128
3104	1		K 2 J (CR25	2322 21	1 73622	4822 110 70128
3105	1		6 K 2 J (CR25	2322 21	1 73622	4822 110 70128
3106	1		K 2 J (CR25	2322 21	1 73622	4822 110 70128
3107	1		5 K 2 J (CR25	2322 21	1 73622	4822 110 70128
3108	1	RESISTOR (AMMOPACK) 6	6 K 2 J (CR25	2322 21	1 73622	4822 110 70128
3109	1		5 K 2 J (CR25	2322 21	1 73622	4822 110 70128
3110	1			CR25	2322 21		4822 110 70128 4822 110 70128
3111	1			CR25	2322 21		4822 110 70128
3112	1			CR25	2322 21 2322 21		4822 110 70128
3113	1			CR25 CR25	2322 21		4822 110 70128
3114	1			CR25	2322 21		4822 110 70128
3115	1			CR25	2322 21		4822 110 70128
3116	1	•		CR25		1 73302	4822 110 70119
3117	1			CR25		1 73302	4822 110 70119
3118	1	•		CR25		1 73302	4822 110 70119
3119	1						
3120	1	•	3 K J			1 73302	4822 110 70119
3121	1	•		CR25	2322 21		4822 110 70119
3122	1	· · · · · · · · · · · · · · · · · · ·		CR25	2322 21		4822 110 70119
3123	1	•		CR25	2322 21		4822 110 70119
3124	1	•		CR25		1 73302	4822 110 70119
3125	1			CR25	2322 21		4822 110 70119
3126	1	•		CR25	2322 21		4822 110 70119
3127	1	•		CR25		1 73302	4822 110 70119
3128	1	•		CR25		1 73302	4822 110 70119
3129	1	RESISTOR (AMMOPACK) 3	3 K J	CR25	2322 21	1 73302	4822 110 70119
3130	1	RESISTOR (AMMOPACK) 3	3 K J	CR25	2322 21	1 73302	4822 110 7011 9
3131	1			CR25		1 73302	4822 110 70119
3132	1			CR25	2322 21	1 73302	4822 110 70119
3133	1	•		CR25		1 73302	4822 110 70119
3134	1			CR25	2322 21	1 73302	4822 110 70119

1983-10-14

SPARE PART CATALOGUE IEEE-BOARD



ITEM	QTY	DESCRIPTION	CODE	NUMBER	SERVICE NUMBER
7101	1	I.C. 74 S 38 N	9332	920 50112	5322 209 85677
7102	1	I.C. 74 LS 240 N (TI) 9334	182 20682	5322 209 85862
7103	1	I.C. 74 LS 273	9334	121 80112	5322 209 85792
7104	1	I.C. 74 LS 245 N (TI) 9336	628 70682	5322 209 86225
7105	1	I.C. 74 S 38 N	9332	920 50112	5322 209 85677
7106	1	I.C. 74 S 38 N	9322	920 50112	5322 209 85677
7107	1	I.C. 74 LS 30 A	9332	870 80112	5322 209 84985
7108	1	I.C. 74 S 38 N	9332	920 50112	5322 209 85677
7 109	1	I.C. 74 LS 240 N	9334	201 20112	5322 209 85862
7110	1	I.C. 74 LS 273	9334	121 80112	5322 209 85792
7111	1	I.C. 74 LS 139 N	9332	873 60112	5322 209 85839
7112	1	I.C. 74 LS 08 A	9332	869 50112	5322 209 84995



SPARE PART CATALOGUE 4x64k RAM-BOARD

ITEM	QTY	DESCRIPTION		CODE NU	JMBER SERVICE NUMBER
1 ,	1	4x64k RAM BOAR	RD PCB ASSY	5103 108 0	02970 * 5103 109 30050
2001 2002 2003 2004 2005 2006	1 1 1 1 1	CER-CAP CL.1 CER-CAP CL.1 CER-CAP CER-CAP EL-CAP CER-CAP	100 N S 63 V SI 33 M 16 V	2222 679 7 2222 679 7 2M. 2012 572 1 2012 572 1 2222 035 3 2M. 2012 572 1	70391 * 5103 109 30570 10028 * 5103 109 30600 10028 * 5103 109 30600 35339 4822 124 40272 10028 * 5103 109 30600
2007 2008 2009	1 1 1	CER-CAP CER-CAP CER-CAP	100 N S 63 V SI	EM. 2012 572 1 EM. 2012 572 1 EM. 2012 572 1	10028 * 5103 109 30600
2010 2011 2012 2013 2014 2015 2016 2017 2018	1 1 1 1 1 1 1	CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP	100 N S 63 V SII 100 N S 63 V SII	EM. 2012 572 1	10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600
2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029	1 1 1 1 1 1 1 1 1	CER-CAP	100 N S 63 V SI 100 N S 63 V SI	EM. 2012 572 1 EM. 2012 572 1	10028 * 5103 109 30600 10028 * 5103 109 30600
2030 2031 2032 2033 2034 2035 2036 2037 2038 2039	1 1 1 1 1 1 1 1 1	CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP	100 N S 63 V SII 100 N S 63 V SII	EM. 2012 572 1 EM. 2012 572 1	10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600
2040 2041 2042 2043 2044 2045	1 1 1 1 1	CER-CAP CER-CAP CER-CAP CER-CAP CER-CAP EL-CAP	100 N S 63 V SII 100 N S 63 V SII 100 N S 63 V SII	EM. 2012 572 1 2222 035 3	10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600 10028 * 5103 109 30600

1983-10-14

SPARE PART CATALOGUE 4x64k RAM-BOARD



ITEM	QTY	DESCRIPTION	CODE	NUMBER	SERVICE NUMBER
3001 3002 3003	1 1 1	RESISTOR (AMMOPACK) 100 R J CR25 RESISTOR (AMMOPACK) 220 R J CR25 RESISTOR (AMMOPACK) 100 R J CR25	2322 21 2322 21 2322 21	1 73221	4822 110 73081 4822 110 73089 4822 110 73081
4001 4002 4003	1 1 1	RES NETWORK 898-3-R22 RES NETWORK 4310R-101-561 (BOURNS) RES NETWORK 898-3-R22	2122 118 2122 118 2122 118	8 00734 *	5322 111 94266 5103 109 30840 5322 111 94266
5001	1	COIL ASSY	5103 10	8 20270 *	5103 109 30910



SPARE PART CATALOGUE 4x64k RAM-BOARD

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1984-04-14

ITEM	QTY	DESCR	IPTION		CODE	NUMBER	SERVICE NUMBER
7001	1	I.C.	74 LS 11		9332	869 80112 3	5103 109 31060
7002	1	I.C.	74 S 123	N (7002) R	AM 5103	108 52370	5103 109 31150
7003	1	I.C.	74 LS 174	В		874 80112	4822 209 50008
7004	1	I.C.	74 LS 244		9334	307 60112	5322 209 86017
7005	1	I.C.	74 S 00	N	9332	813 80112	5322 209 84167
7006	1	I.C.	74 S 04	N		617 40112	5322 209 84475
7007	1	I:C.	74 LS 02	A		886 70112	5322 209 85312
7008	1	I.C.	74 S 00	N		813 80112	5322 209 84167
7009	1	I.C.	74 LS 30	A	9332	870 80112	5322 209 84985
7010	1	I.C.	82 S 129	N (7010) R			5103 109 31160
7011	1	I.C.	82 S 126	N (7011) R	RAM 5103	108 52520	* 5103 109 31170
7012	1	I.C.	74 S 157	N	9332	878 90112	5322 209 85669
7013	1	I.C.	74 S 157	N		878 90112	5322 209 85669
7014	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7015	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7016	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7017	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7018	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7019	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7020	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7021	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7022	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7023	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7024	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7025	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7026	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7027	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7028	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7029	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7030	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7031	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7032	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7033	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7034	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7035	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7036	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7037	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7038	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7039	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977
7040	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7041	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7042	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7043	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7044	1	I.C.	HM 4864-2	(HITJ)		043 10682	5322 209 80977
7045	1	I.C.	HM 4864-2	(HITJ)	9336	043 10682	5322 209 80977

SPARE PART CATALOGUE 4x64k RAM-BOARD



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SPARE PART CATALOGUE MISCELLANEOUS PARTS

ITEM	QTY	DESCRIPTION	CODE	NUMBER	SERVICE NUMBER
33 38 42 42 55	1 1 1 1	POWER SUPPLY UNIT MONITOR MONOCHROME GREEN FLOPPY DISK UNIT 160K FLOPPY DISK UNIT 640K DISTRIBUTION BOARD ASSY	5103 1 5103 1 5103 1	.08 73540 .08 73530 .08 52260 .08 73680 .08 02730	* 5103 109 30100 * 5103 109 30110 * 5103 109 30120 * 5103 109 30130 * 5103 109 30020
		HOUSING			
51 70 72 45 46	1 1 1 1	FRONT MASK REAR MASK CASE COVER BOTTOM PLATE RUBBER FOOT	5103 1 5103 1 5103 1	.07 59600 .04 18660 .07 59790 .04 18620 .04 40940	* 5103 109 30200 * 5103 109 30210 * 5103 109 30220 * 5103 109 30230 * 5103 109 30240

SPARE PART CATALOGUE MISCELLANEOUS PARTS



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A

P 2000 C CHARACTER GENERATOR LISTING

				UNDERTHED
CHARACTER	CHARACTER	GENERATOR	ROM CONTENTS	UNDEFINED
00	FF FF FF FF	FF FF FF FF	FF FF FF FF	xx xx xx xx
01	FO FO FO FO	FF FF FF FF		xx xx xx xx
02	OF OF OF OF	FF FF FF FF		xx xx xx xx
03	00 00 00 00	FF FF FF FI		xx xx xx xx
04	FF FF FF FF	FO FO FO FO		xx xx xx xx
05	FO FO FO FO	FO FO FO FO	FF FF FF	xx xx xx xx
06	OF OF OF OF	FO FO FO FO		xx xx xx xx
07	00 00 00 00	FO FO FO FO	FF FF FF FF	xx xx xx xx
•				
- 08	FF FF FF FF	OF OF OF O	F FF FF FF	XX XX XX XX
09	FO FO FO FO	OF OF OF OI	F FF FF FF	XX XX XX XX
OA	OF OF OF OF	OF OF OF O	F FF FF FF	XX XX XX XX
ОВ	00 00 00 00	OF OF OF O	F FF FF FF	xx xx xx xx
0C	FF FF FF FF	00 00 00 00	O FF FF FF FF	xx xx xx xx
OD	FO FO FO FO	00 00 00 00	O FF FF FF FF	XX XX XX XX
OE	OF OF OF OF	00 00 00 00	O FF FF FF FF	xx xx xx xx
OF	00 00 00 00	00 00 00 00	O FF FF FF FF	xx xx xx xx
				,
10	FF FF FF FF	FF FF FF F		xx xx xx xx
11	FO FO FO FO	FF FF FF F		xx xx xx xx
12	OF OF OF OF	FF FF FF F		xx xx xx xx
13	00 00 00 00	FF FF FF F		xx xx xx xx
14	FF FF FF FF	FO FO FO	-	xx xx xx xx
15	FO FO FO FO	FO FO FO FO		xx xx xx xx
16	OF OF OF OF	FO FO FO FO	-	XX XX XX XX
17	00 00 00 00	FO FO FO	o fo fo fo	XX XX XX XX
18	FF FF FF FF	OF OF OF O	F FO FO FO	xx xx xx xx
19	FO FO FO FO	OF OF OF O		XX XX XX XX
1A	OF OF OF OF	OF OF OF O		xx xx xx xx
1 B	00 00 00 00	OF OF OF O		xx xx xx xx
1C	FF FF FF FF	00 00 00 0		xx xx xx xx
1 D	FO FO FO FO	00 00 00 0		xx xx xx xx
1E	OF OF OF OF	00 00 00 0		xx xx xx xx
1F	00 00 00 00	00 00 00 0		xx xx xx xx
20	FF FF FF FF	FF FF FF F	F FF FF FF	xx xx xx xx
21	FF E7 E7 E7	E7 E7 FF E		xx xx xx xx
22	FF DB DB DB	FF FF FF F	FF FF FF FF	xx xx xx xx
23	FF DB 81 DB	DB 81 DB F	F FF FF FF	xx xx xx xx
24	FF E7 83 E5			xx xx xx xx
25	FF F9 B9 DF	EF F7 9B 9		xx xx xx xx
26	FF F3 ED F3	F5 AD 9D 8		
27	FF F7 F7 F7	FF FF FF F	FF FF FF FF	xx xx xx xx



CHARACTER	CHARACTER	GENERATOR ROM	d CONTENTS	UNDEFINED
28	DE ED D7 DD	77 77		
29	FF EF F7 FB FF F7 EF DF	FB FB F7 EF DF DF EF F7	FF FF FF FF	XX XX XX XX
2A	FF FF D5 E3	C1 E3 D5 FF	FF FF FF FF FF FF FF FF	XX XX XX XX
2 B	FF FF F7 F7	C1 E3 D3 FF C1 F7 F7 FF	FF FF FF FF	XX XX XX XX
2C	FF FF FF FF	FF FF EF EF	EF F7 FF FF	XX XX XX XX
2 D	FF FF FF FF	C3 FF FF FF	FF FF FF FF	XX XX XX XX
2E	FF FF FF FF	FF FF E7 E7	FF FF FF FF	XX XX XX XX
2F	FF FF BF DF	EF F7 FB FD	FF FF FF FF	XX XX XX XX
30	FF C3 BD BD	BD BD BD C3	FF FF FF FF	xx xx xx xx
31	FF DF CF D7	DF DF DF 8F	FF FF FF FF	XX XX XX XX
32	FF C3 BD BF	CF F7 FB 81	FF FF FF FF	XX XX XX XX
33	FF C3 BD BF	CF BF BD C3	FF FF FF FF	XX XX XX XX
34	FF DF CF D7	DB 81 DF DF	FF FF FF FF	xx xx xx xx
35	FF 81 FD C1	BF BF BD C3	FF FF FF FF	xx xx xx xx
36	FF C3 BD FD	C1 BD BD C3	FF FF FF FF	xx xx xx xx
37	FF 81 BF DF	EF F7 FB FB	FF FF FF FF	xx xx xx xx
38	FF C3 BD BD	C3 BD BD C3	FF FF FF FF	xx xx xx xx
39	FF C3 BD BD	83 BF BD C3	FF FF FF FF	xx xx xx xx
3A	FF FF FF F7	FF F7 FF FF	FF FF FF FF	xx xx xx xx
3B	FF FF FF FF	EF FF EF EF	EF F7 FF FF	xx xx xx xx
3C	FF FF F7 FB	FD FB F7 FF	FF FF FF FF	xx xx xx xx
3D	FF FF FF C3	FF C3 FF FF	FF FF FF FF	xx xx xx xx
3E	FF FF F7 EF	DF EF F7 FF	FF FF FF FF	xx xx xx xx
3F	FF C3 BD BF	CF F7 FF F7	FF FF FF FF	xx xx xx xx
40	FF FF FF C3	BD 85 B5 85	FD C3 FF FF	xx xx xx xx
41	FF E7 DB BD	BD 81 BD BD	FF FF FF FF	XX XX XX XX
42	FF C1 BD BD	C1 BD BD C1	FF FF FF FF	XX XX XX XX
43	FF C3 BD FD	FD FD BD C3	FF FF FF FF	XX XX XX XX
44	FF C1 BD BD	BD BD BD C1	FF FF FF FF	xx xx xx xx
45	FF 81 FD FD	C1 FD FD 81	FF FF FF FF	xx xx xx xx
46	FF 81 FD FD	C1 FD FD FD	FF FF FF FF	xx xx xx xx
47	FF C3 BD FD	8D BD BD 83	FF FF FF FF	xx xx xx xx
48	FF BD BD BD	81 BD BD BD	FF FF FF FF	xx xx xx xx
49	FF C7 EF EF	EF EF EF C7	FF FF FF FF	xx xx xx xx
4A	FF 81 BF BF	BF BF BD C3	FF FF FF FF	xx xx xx xx
4B	FF BD DD ED	F5 E9 DD BD	FF FF FF FF	xx xx xx xx
4C	FF FD FD FD	FD FD FD 81	FF FF FF FF	xx xx xx xx
4D	FF BD 99 A5	A5 BD BD BD	FF FF FF FF	xx xx xx xx
4E	FF BD B9 B5	AD 9D BD BD	FF FF FF FF	XX XX XX XX
4 F	FF 81 BD BD	BD BD BD 81	FF FF FF FF	xx xx xx xx



CHARACTER	CHARACTER	GENERATOR	ROM CONTENTS	UNDEFINED
50	FF C1 BD BD	C1 FD FD	FD FF FF FF FF	xx xx xx xx
50			81 FF FF FF FF	XX XX XX XX
51		C1 ED DD		
52	FF C1 BD BD FF C3 BD FB	E7 DF BD	C3 FF FF FF FF	
53		F7 F7 F7	F7 FF FF FF FF	
54		BD BD BD		
55	FF BD BD BD FF BD BD BD	BD BD DB		
56	· -	A5 A5 99	_,	
57	FF BD BD BD	אל כא כא	עם	
58	FF BD DB E7	E7 DB BD		
59	FF BD BD DB	E7 F7 F7	F7 FF FF FF	XX XX XX XX
5A	FF 81 BF DF	EF F7 FB	81 FF FF FF FF	XX XX XX XX
5B	FF C3 FB FB	FB FB FB	C3 FF FF FF FF	xx xx xx xx
5 C	FF FF FD FB	F7 EF DF	BF FF FF FF FF	XX XX XX XX
5D	FF C3 DF DF	DF DF DF	C3 FF FF FF FI	XX XX XX XX
5E	FF F7 EB DD	FF FF FF	FF FF FF FF	XX XX XX XX
5F	FF FF FF FF	FF FF FF	81 FF FF FF FF	XX XX XX XX
31				
60	FF F7 EF DF	FF FF FF		
61	FF FF FF A3	9D BD 9D		
62	FF FD FD C5	B9 BD BD		
63	FF FF FF C3	BD FD BD		
64	FF BF BF A3	9D BD 9D		
65	FF FF FF C3		C3 FF FF FF F	
66	FF CF B7 F7	81 F7 F7	$\mathbf{F7}$ $\mathbf{F7}$ $\mathbf{F7}$ \mathbf{FF} $\mathbf{F1}$	XX XX XX XX
67	FF FF FF A3	9D BD 9D	A3 BF BD C3 FI	XX XX XX XX
	FF FD FD C5	B9 BD BI	BD FF FF FF F	F xx xx xx xx
68 69	FF EF FF E7		C7 FF FF FF FI	
	FF DF FF DF	DF DF DF		
6A 6B	FF FD FD DD	ED F5 E9	***	
6C	FF FD FD FD	FD FD DI		
6D	FF FF FF D5	A9 AD AI		
6E	FF FF FF C5	B9 BD BI		
6F	FF FF FF C3	BD BD BI		
Or	FF FF FF C5	טם שם שם	, 05 11 11 11 1.	
70	FF FF FF C5	B9 BD B9		
71	FF FF FF A3	9D BD 91		
72	FF FF FF C5	B9 FD FI		
73	FF FF FF 83			
74	FF FB FB C1	FB FB Bl		F xx xx xx xx
75	FF FF FF BD	BD BD BI		F xx xx xx xx
76	FF FF FF BD			
77	FF FF FF BD	BD A5 A	5 DB FF FF FF F	F xx xx xx xx

4



CHARACTER	CHARACTER	GENERATOR R	CONTENTS	UNDEFINED
78	FF FF FF BD	DB E7 DB BD	वद वद वद वद	
76 79	FF FF FF BD	DB E7 F7 FB	FF FF FF FF FD FF FF FF	XX XX XX XX
7 A	FF FF FF 81	DF E7 FB 81	FF FF FF FF	XX XX XX XX
7 B	FF F7 FB FB	FD FB FB F7	FF FF FF FF	XX XX XX XX
7 C	FF F7 F7 F7	F7 F7 F7 F7	FF FF FF FF	
7 D	FF F7 EF EF	DF EF EF F7	FF FF FF FF	XX XX XX XX XX
7 E	FF B3 CD FF	FF FF FF FF	FF FF FF FF	XX XX XX XX
7 F	FF FF BF B7	BB 81 FB F7	FF FF FF FF	XX XX XX XX
80	FF FF FF FF	FF FF FF FF	OF OF OF OF	xx xx xx xx
81	FO FO FO FO	FF FF FF FF	OF OF OF OF	XX XX XX XX
82	OF OF OF OF	FF FF FF FF	OF OF OF OF	XX XX XX XX
83	00 00 00 00	FF FF FF FF	OF OF OF OF	XX XX XX XX
84	FF FF FF FF	FO FO FO FO	OF OF OF OF	XX XX XX XX
85	FO FO FO FO	FO FO FO FO	OF OF OF OF	XX XX XX XX
86	OF OF OF OF	FO FO FO FO	OF OF OF OF	xx xx xx xx
87	00 00 00 00	FO FO FO FO	OF OF OF OF	xx xx xx xx
88	FF FF FF FF	OF OF OF OF	OF OF OF OF	VV vvv 3/20 2020
89	FO FO FO FO	OF OF OF OF	OF OF OF OF	XX XX XX XX
8A	OF OF OF OF	OF OF OF OF	OF OF OF OF	XX XX XX XX
8B	00 00 00 00	OF OF OF OF	OF OF OF OF	XX XX XX XX
8C	FF FF FF FF	00 00 00 00	OF OF OF OF	XX XX XX XX
8D	FO FO FO FO	00 00 00 00	OF OF OF OF	XX XX XX XX
8E	OF OF OF OF	00 00 00 00	OF OF OF OF	XX XX XX XX
8F	00 00 00 00	00 00 00 00	OF OF OF OF	XX XX XX XX
90	FF FF FF FF	FF FF FF FF	00 00 00 00	
91	FO FO FO FO	FF FF FF FF	00 00 00 00	XX XX XX XX
92	OF OF OF OF	FF FF FF FF	00 00 00 00	XX XX XX XX
93	00 00 00 00	FF FF FF FF	00 00 00 00	XX XX XX XX
94.	FF FF FF FF	FO FO FO FO	00 00 00 00	XX XX XX XX
95	FO FO FO FO	FO FO FO FO	00 00 00 00	XX XX XX XX
96	OF OF OF OF	FO FO FO FO	00 00 00 00	XX XX XX XX
97	00 00 00 00	FO FO FO FO	00 00 00 00	xx xx xx xx
98	नव वच वच वच		00 00 00 00	
	FF FF FF FF	OF OF OF OF	00 00 00 00	XX XX XX XX
99 9A	FO FO FO FO OF OF	OF OF OF OF OF OF	00 00 00 00	XX XX XX XX
9B	00 00 00 00	OF OF OF OF	00 00 00 00 00 00 00 00	XX XX XX XX
9C	FF FF FF FF	00 00 00 00	00 00 00 00	XX XX XX XX
9D	FO FO FO FO	00 00 00 00	00 00 00 00	XX XX XX XX
9E	OF OF OF OF	00 00 00 00	00 00 00 00	XX XX XX XX
9F	00 00 00 00	00 00 00 00	00 00 00 00	XX XX XX XX
) £	00 00 00 00	00 00 00 00	00 00 00 00	XX XX XX XX



CHARACTER	CHARACTER	GENERATOR	ROM CO	NTENTS	UNDEFINED
AO	FF F7 EB DD	EB F7 FF	FF FF FF	FF FF	xx xx xx xx
Al	FF E7 FF E7		E7 FF FF	FF FF	xx xx xx xx
A2	FF FF BF C3	AD F5 B9	C1 FF FE		xx xx xx xx
A3	FF C7 BB FB	E1 FB BB	C5 FF FF	FF FF	xx xx xx xx
A4	B3 CD FF 81	BD BD BD	81 FF FF	FF FF	xx xx xx xx
A5	FF BD BD DB	E7 F7 C1	F7 FF FI	F FF FF	XX XX XX XX
A6	FF DB FF FF	FF FF FF	FF FF FI	F FF FF	xx xx xx xx
A7	FF C3 FD C3	BD C3 BF	C1 FF FI	F FF FF	xx xx xx xx
A8	FF BD C3 DB	DB C3 BD			xx xx xx xx
A9	FF FF FF FF	FF 07 F7			xx xx xx xx
AA	F7 F7 F7 F7	F7 07 FF			xx xx xx xx
AB	FF FF B7 DB	ED DB B7		F FF FF	xx xx xx xx
AC	FF FF FF F7	FB 81 FB		F FF FF	xx xx xx xx
AD	FF F7 E3 D5	F7 F7 F7		F FF FF	xx xx xx xx
AE	FF FF FF EF	DF 81 DF		F FF FF	xx xx xx xx
AF	FF F7 F7 F7	F7 D5 E3	F7 FF F	F FF FF	xx xx xx xx
во	FF C7 BB BB	C7 FF FF		F FF FF	xx xx xx xx
B1	FF F7 F7 C1	F7 F7 FF		F FF FF	XX XX XX XX
B2	CF B7 DF EF	87 FF FF		F FF FF	XX XX XX XX
В3	CF B7 DF B7	CF FF FF		F FF FF	XX XX XX XX
B4	FF FF BB D7	EF D7 BB			XX XX XX XX
B5	FF FF FF BB	BB BB BB		B FB FF	XX XX XX XX
B6	FF D3 D1 D1	D3 D7 D7		F FF FF F FF FF	XX XX XX XX
В7	B3 CD FF C3	BD BD BD	C) FF F.	c ee ee	XX XX XX XX
В8	FF FF FF F7	FF C1 FF	F7 FF F	F FF FF	xx xx xx xx
В9	FF FF FF FF	FF FO F7		7 F7 F7	xx xx xx xx
BA	F7 F7 F7 F7	F7 FO FF			xx xx xx xx
ВВ	FF FF ED DB			F FF FF	xx xx xx xx
BC	FB F9 7A BB	DB EF B7			xx xx xx xx
BD	FB F9 7A BB	DB EF B7			xx xx xx xx
BE	F9 F6 7B B6	D9 EF B7			xx xx xx xx
BF	FF EF FF EF	F3 FD BD	C3 FF F	F FF FF	xx xx xx xx
CO	FF 7F BF 81	EF 81 FB		F FF FF	xx xx xx xx
C1	EF F7 FF C3	BD BD 81		F FF FF	XX XX XX XX
C2	FF EF F7 FB	FF FF FF		F FF FF	XX XX XX XX
C3	F7 EF FF C3	BD BD 81		F FF FF	xx xx xx xx
C4	E7 DB FF C3	BD BD 81		F FF FF	XX XX XX XX
C5	DB FF C3 BD	BD 81 BD		F FF FF	XX XX XX XX
C6	EF F7 FF 81	FD C1 FD		F FF FF	XX XX XX XX
C7	F7 EF FF 81	FD C1 FD	OT LL L	F FF FF	XX XX XX XX

6



CHARACTER	CHARACTER	GENERATOR ROM	CONTENTS	UNDEFINED
C8	E7 DB FF 81	ED (1) ED (1)		
C9	F7 F7 F7 F7	_	FF FF FF FF F7 F7 F7	XX XX XX XX
CA	FF FF FF FF		- · - · - · - ·	XX XX XX XX
CB	DF EF FF C7		F7 F7 F7 F7 FF FF FF FF	XX XX XX XX
CC	F7 EF FF C7		FF FF FF FF	XX XX XX XX
CD	FF EB FF E3		FF FF FF FF	XX XX XX XX
CE	FF C3 BD FD		EF DF E7 FF	XX XX XX XX
CF	B3 CD FF B9		FF FF FF FF	XX XX XX XX
		23 122 70 20		AA AA AA AA
DO	FF FF FF FF	FF OO FF FF	FF FF FF FF	xx xx xx xx
D1	EF F7 FF A3	9D BD 9D A3	FF FF FF FF	XX XX XX XX
D2	F7 EB FF F3	F7 F7 F7 E3	FF FF FF FF	xx xx xx xx
D3	F7 EF FF A3	9D BD 9D A3	FF FF FF FF	xx xx xx xx
D4	E7 DB FF A3	9D BD 9D A3	FF FF FF FF	xx xx xx xx
D5	FF DB FF A3	9D BD 9D A3	FF FF FF FF	xx xx xx xx
D6	EF F7 FF C3		FF FF FF FF	xx xx xx xx
D7	F7 EF FF C3	BD 81 FD C3	FF FF FF FF	xx xx xx xx
D8	E7 DB FF C3	BD 81 FD C3	FF FF FF FF	xx xx xx xx
D9	F7 F7 F7 F7	[[.]	F7 F7 F7 F7	XX XX XX XX
DA	F7 F7 F7 F7		FF FF FF FF	XX XX XX XX
DB	F7 FB FF F3		FF FF FF FF	XX XX XX XX
DC	FB F7 FF F3	F7 F7 F7 E3	FF FF FF FF	xx xx xx xx
DD	FF EB FF F3	F7 F7 F7 E3 I	FF FF FF FF	xx xx xx xx
DE	FF FF FF E3		F7 EF F3 FF	xx xx xx xx
DF	B3 CD FF C5	B9 BD BD BD I	FF FF FF FF	xx xx xx xx
EO	FF C3 BD BD	BD DB DB 99	FF FF FF FF	xx xx xx xx
E1	FF O3 ED ED		FF FF FF FF	XX XX XX XX
E2 -	E7 DB E7 DB		F FF FF FF	XX XX XX XX
E3	FF A3 9D 9D		F FF FF FF	XX XX XX XX
E4	F7 EB FF 81		F FF FF FF	XX XX XX XX
E5 /	DB FF 81 BD		F FF FF FF	XX XX XX XX
E6	EF F7 FF 81		F FF FF FF	XX XX XX XX
E7	F7 EF FF 81		FF FF FF FF	xx xx xx xx
E8	EF F7 BD BD	BD BD BD C3 F	FF FF FF FF	
E9	7F 81 9D AD			XX XX XX XX
EA	F7 F7 F7 F7			XX XX XX XX
EB	FF C3 BD BD		?7 F7 F7 F7 ?F FF FF FF	XX XX XX XX
EC	F7 EF BD BD		F FF FF FF	XX XX XX XX
ED	DB FF BD BD		FF FF FF FF	XX XX XX XX
EE	B3 CD FF C3	_	F FF FF FF	XX XX XX XX
EF	FF FF FF C3		F FF FF FF	XX XX XX XX





CHARACTER	CHARACTER	GENERATOR	ROM CONTENTS	UNDEFINED
FO	FF DB FF C3	BD 91 FD (C3 FF FF FF FF	XX XX XX XX
F1	FF FF FF C9	B7 C1 F6	C9 FF FF FF	XX XX XX XX
F2	E7 DB E7 A3	9D BD 9D A	A3 FF FF FF FF	XX XX XX XX
F3	F7 EB FF DD	DD DD DD	E3 FF FF FF	xx xx xx xx
F4	E7 DB FF C3	BD BD BD	C3 FF FF FF .FF	XX XX XX XX
F5	FF DB FF C3	BD BD BD	C3 FF FF FF FF	XX XX XX XX
F6	EF F7 FF C3	BD BD BD	C3 FF FF FF FF	XX XX XX XX
F7	F7 EF FF C3	BD BD BD	C3 FF FF FF	xx xx xx xx
F8	EF F7 FF BD	BD BD BD	C3 FF FF FF FF	xx xx xx xx
F9	FF FF BF C3	_	C1 FE FF FF FF	xx xx xx xx
FA	F7 F7 F7 F7		F7 F7 F7 F7	xx xx xx xx
FB	FF C3 BD BD	CD BD BD	CD FD FF FF FF	xx xx xx xx
FC	FF F7 EF BD	BD BD BD	C3 FF FF FF FF	xx xx xx xx
FD	FF DB FF BD	BD BD BD	C3 FF FF FF FF	xx xx xx xx
FE	B3 CD FF A3	9D BD 9D	A3 FF FF FF FF	xx xx xx xx
FF	FF FF FF E7	E7 FF FF	FF FF FF FF	xx xx xx xx



Basic Program Using Polar Co-ordinates

В

USING POLAR CO-ORDINATES

```
10 ' THIS PROCEDURE USES DIRECT CONOUT 20 ' XY% WRITES 2 BYTE X COORDINATE AND 1 BYTE Y COORDINATE
40 '
                                        C,(HL) ;GET X LOW BYTE OUTBYTE DOOF
                                LD
50 DATA &H4E:'
                                CALL
60 DATA &HCD, &HOE, &HDO:'
                                        HL
                                INC
70 DATA &H23:'
                                        C,(HL) ;GET X HIGH BYTE OUTBYTE
                                LD
80 DATA &H4E:'
90 DATA &HCD, &HOE, &HDO:'
                                CALL
                                        DE, HL
100 DATA &HEB:'
                                EX
                                        OUTBYTE; GET Y
110 DATA &H4E:'
                                LD
120 DATA &HC3, &HOE, &HDO:'
                                JP
130 '
                       OUTBYTE: PUSH
140 DATA &HE5:'
                                        DE
                                PUSH
150 DATA &HD5:'
                                         HL,(1) ;CBIOS JUMP TABLE ADDR.
160 DATA &H2A,1,0:'
                                LD
                                                 OFFSET TO CONOUT
                                LD
                                         DE,9
170 DATA &H11,9,0:
                                         HL, DE
                                 ADD
180 DATA &H19:'
                                         DE, RETX ; RETURN ADDRESS FOR CONOUT
190 DATA &H11,&H1C,&HDO:'
                                 LD
200 DATA &HD5:'
210 DATA &HE9:'
                                 PUSH
                                         DE
                                         (HL)
                                                 ;CALL CONOUT
                                 .IP
                                 POP
                                         DE
                        RETX:
220 DATA &HD1:'
                                         HL
230 DATA &HE1:'
                                 POP
                                 RET
240 DATA &HC9:1
250 DATA &HFF
260 '--
270 XY=&HD000
 280 CLEAR , XY, 250
 290 XY=&HD000
 300 I%=0
 310 WHILE+ K%->&HFF
          READ K%: POKE &HD000+1%, K%: 1%=1%+1
 320
 330 WEND
 340 ' THIS PROCEDURE USES DIRECT CONOUT
 350 ' XY% WRITES 2 BYTE ANGLE AND 2 BYTE ABS. VALUE
 370 '
                                         C,(HL) ;GET X LOW BYTE OUTBYTE
 380 DATA &H4E:'
                                 LD '
                                 CALL
 390 DATA &HCD, &H10, &HD1:
                                 INC
                                         HL
 400 DATA &H23:
                                         C,(HL) ;GET X HIGH BYTE
                                 LD
 410 DATA &H4E:
                                         OUTBYTE
 420 DATA &HCD, &H10, &HD1:
                                 CALL
                                 EX
                                         DE, HL
 430 DATA &HEB: '
                                                 GET Y
                                         C,(HL)
                                 LD
 440 DATA &H4E:'
                                         OUTBYTE
 450 DATA &HCD, &H10, &HD1:'
                                 CALL
 460 DATA &H23,&H4E:'
                                 INC HL + LD C, (HL)
                         OUTBYTE: PUSH
                                        HI.
 480 DATA &HD5:'
                                 PUSH
                                         DE
                                         HL,(1) ;CBIOS JUMP TABLE ADDR.
                                 LD
 490 DATA &H2A,1,0:'
                                                 OFFSET TO CONOUT
                                 LD
                                         DE,9
 500 DATA &H11,9,0:
                                         HL, DE
                                 ADD
 510 DATA &H19:
```

2

Basic Program Using Polar Co-ordinates



```
520 DATA &H11,&H1E,&HD1:'
530 DATA &HD5:'
                                           LD
PUSH
                                                      DE, RETX ; RETURN ADDRESS FOR CONOUT
                                                      DE
540 DATA &HE9:
                                           JP.
                                                      (HL)
                                                                ; CALL CONOUT
550 DATA &HD1:'
                                RETX:
                                           POP
                                                      DE
560 DATA &HE1:'
                                           POP
                                                      HL
570 DATA &HC9:'
                                           RET
580 DATA &HFF
590 '-
600 PXY=&HD100
610 I%=0:K%=0
620 WHILE+ KX==&HFF
             READ K%: POKE &HD100+I%, K%: I%=I%+1
640 WEND
650 WIDTH 255:PRINT CHR$(12)+CHR$(27)+"3";
660 OG$=CHR$(27)+"z":MT$=CHR$(27)+"y":DT$=CHR$(27)+"U"
670 FOR OXZ=80 TO 450 STEP 120 ' DISTANCE IN X-AXIS
680 FOR OYZ=50 TO 200 STEP 120 ' DISTANCE IN Y-AXIS
690 PRINT OG$;:CALL XY(OX%,OY%)
700 GOSUB 750
710 NEXT
720 NEXT
730 REM -
740 K$=INKEY$:IF K$="" THEN 740 ELSE PRINT CHR$(27)+"4":END
750 REM
760 AB%=50
770 FOR A%=0 TO 360 STEP 60
780 PRINT MT$;:CALL PXY(A%,AB%)
790 AX%=A%
800 FOR I%=1 TO 3 '
                                             NUMBER OF TURNS
810 AX%=AX%+90:PRINT-DT$;:CALL PXY(AX%, AB%)
820 NEXT
830 NEXT
840 RETURN
```

Manual Status Control Form

P2000C SYSTEM REFERENCE AND SERVICE MANUAL

12 NC: 5103 993 30422

This issue comprises the following updates:

Amendment List 1

Significant changes to the text (or illustrations) are marked with a line in the outer margin.

The deletion of text is marked with '*'.

•

Manual Comment Form

	P2000C SY	STEM REFE	RENCE AND	SERVICE	MANUAL		
	12 NC: 5	103 993 3	0422				
	Including	updates:	AL1,				
					Origina	tor:	
					Name:	• • • • • • • •	• • • • • • •
					Address	:	• • • • • • •
						• • • • • • •	• • • • • • •
						• • • • • • •	• • • • • • •
Comment	(if poss	sible, pomment, ma	olease ac	ld a co n the pro	py of the posed change	page(s)	affected

Please return this form to: Mr J. Stransky - Service Manager
Osterreichische Philips Industrie GmbH
Elekronikfabrik-Microelectronics Wien
Breitenseer Strasse 116
A-1140 WIEN
AUSTRIA



Special Note

The P2000C Maintenance Program is supplied on a 160K Diskette.

To produce a stand-alone Maintenance Diskette (160K or 640K - depending on your system) the following procedure should be followed:

- 1. Place SYSTEM DISKETTE in DRIVE 1
- 2. Place EMPTY 640K (or 160K) FORMATTED DISK in DRIVE 2
- 3. RESET
- 4. Call CONFIG
 - Enter SYSTEM CONFIGURATION (1) and select appropriate configuration. Press "Carriage Return".
 - Set CAPSLOCK and PRINTER TIMEOUT as required.
 - Enter AUTOSTART STRING as MN11.
 - Enter MESSAGE as required.
 - Enter 2 for FLOPPY DRIVE TO WRITE NEW SYSTEM CONFIRM
- 5. RESET
- 6. Call UTIL
 - Define LANGUAGE AND FLOPPY ARRANGEMENT (POINT 4)
 - Select appropriate Drives.
 - The MENU will be displayed.
 - Select COPY FLOPPY
 - Enter SOURCE = 1 DESTINATION = 2
 - Enter "YES" to Verify.
 - Select SOURCE DISK TYPE 2 (160K)
 - ° Select SYSTEM = CP/M

!!! REMOVE SYSTEM DISK AND INSERT 160K MN11 IN DRIVE 1 !!!

- PRESS ANY KEY
- Enter N(o) to NEXT COPY
- Enter ESC
- 7. Remove and store the 160K diskette from DRIVE 1 (MN11).
- 8. The diskette in DRIVE 2 is your Maintenance Diskette and may be booted in the usual way.



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Preface

PREFACE

This manual describes the internal structure, function and operation of the Philips P2000C Portable Computer. The manual aims to provide the reader with sufficient technical information concerning the standard and optional hardware, the basic input/output operating system (BIOS) and the terminal firmware, so as to allow operation and servicing of the equipment. The manual includes a comprehensive Spare Part Catalogue with instructions for ordering.

The manual covers the anticipated needs of a wide range of readers, from the user who requires a basic understanding of how the system works to the service technician who may need very detailed technical information concerning the hardware of the machine. For this reason some of the information contained in the manual may appear redundant.

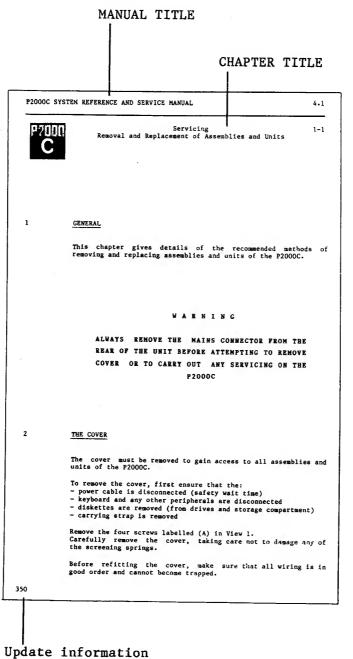
The P2000C uses a number of commercially available integrated circuits, such as the Z80-A CPU, and the reader may find it necessary to consult some of the existing documentation which is available for these products. Where practicable, reference to such documentation has been included in the text.

Preface



Page Layout

This manual has been arranged in four parts with the pages arranged as follows, giving a unique reference to each page:



Part/Chapter numbers
Section/Page numbers



Maintenance Facilities

INTRODUCTION

The maintenance utilities of the P2000C are in three parts:

- 1. Mainboard Test resident in the IPL PROM.
- Terminalboard Test resident in the Terminal ROM.
- The Maintenance Program in CP/M files.

Each part will be described in the following paragraphs.

2 MAINBOARD TEST

2.1 General

At switch-on, a ROM test is carried out and then the Initial Program Load is executed. If this is not successful (if there is no system diskette inserted and/or the hard disk is not at full speed) the message 'SYSTEM DISK?' is displayed.

The MEMORY AND PERIPHERAL DEBUGGER can then be activated by pressing the ESC key.

This situation can also be reached when no system disk is present at CP/M warm boot time by entering 'CTRL-C'. In the first case ASCII keyboard and screen is assumed and the printer speed is 1200 baud, in the second case the values configured on the CP/M system disk are valid.

The aim of this module is to help troubleshooting. Even if booting is impossible, it enables the user to make a short check of memory, ports, floppy disk, hard disk, video, keyboard and printer.



2.2 The Memory and Peripheral Debugger

The program prompt message will be as follows:

'COMMANDS: C,D,DR,DW,F,G,M,P,PS,S,SK

ENTRY: Command Start address End address Other info'

The command code may be followed by a space (not necessary). The separator between the operands may be a space or a comma. An automatic caps-lock function is implemented, i.e., lower case characters cannot be entered.

The syntax is similar to that of the DDT of Digital Research. The command line format differs from that in the P2000 and P2500 Maintenance Program Debugger due to compatibility with Digital Research's Symbolic Debugger.

To exit the debugger, enter the command 'G 0' (zero), 'CR' and any two characters; or simply press the RESET button.

The commands, with examples, are shown below. 'CR' indicates the CARRIAGE RETURN key.

2.2.1 COMMAND C: - COMPARE MEMORY BLOCKS

Example: C 4000 4FFF 5000

This command will compare the block 4000 - 4FFF with the block 5000 - 5FFF. Any differences will be displayed.

2.2.2 COMMAND D: - DISPLAY MEMORY BLOCKS

Example: D 6000 607F

The content of locations 6000 to 607F is displayed (HEX and ASCII).

The program stores the last displayed address and the length of the block. Therefore, to see the next block (6080 to 60FF), the user has only to type D and 'CR'.

D and 'CR' as an initial entry displays the contents of locations 4000 to 40FF. (4000 is the first address of the default disk buffer).

After a disk operation the base address is set to the disk buffer address.

A long display may be stopped and restarted with CTRL-S. Any other character cancels the command.



2.2.3 COMMAND DR: - DISK READ TRACK

Example: DR 126 5000

Reads the contents of drive 1 - track 26 (decimal) to memory locations 5000 to 5FFF.

The first digit indicates the drive number in accordance with the following table:

1 = Floppy-1; first side

2 = Floppy-2; first side

3 = Floppy-3; first side

4 = Floppy-4; first side

5 = Floppy-1; second side

6 = Floppy-2; second side 7 = Floppy-3; second side

8 = Floppy-4; second side

9 = Hard disk-1

The second and third digits give the physical track number in decimal. For floppies this must be between 0 and 79. For hard disk the track number must be between 0 and 99 (i.e., only a small part of the hard disk can be read in this way).

If a destination buffer is not given, location 4000 is assumed.

After issuing this command, a CONTINUOUS read operation is carried out on the designated track until any key is pressed. The result of each read operation is displayed. This will be in the form of 'OK' if the track is read correctly or the uPD765 Floppy Controller RESULT Byte in case of error. For a Hard disk error, this result byte has no significance.

2.2.4 COMMAND DW: - DISK WRITE TRACK

Example: DW 69

Data from locations 4000 to 4FFF is written to Floppy-2; second side, track 9. Drive, side and track information is entered in the same form as for DISK READ TRACK.

2.2.5 COMMAND F: - FILL MEMORY BLOCK WITH ONE BYTE

Example: F 8233 875D 55

The memory locations 8233 to 875D will be filled with 55H.

Maintenance Facilities



2.2.6 COMMAND G: - GO TO AN ADDRESS (CALL A PROGRAM)

Example: G 5000

The user can enter small programs with the S(et) command (starting at location 5000 in the example) and execute them with the 'G' command. The C9 (RET) instruction at the end of the user program leads back to the Debugger.

2.2.7 COMMAND M: - MOVE MEMORY BLOCK

Example: M 4000 4FFF 5000

The block 4000 - 4FFF is copied to 5000 - 5FFF.

2.2.8 COMMAND P: - PORT READ/WRITE

Example: P 2A

The port 2A is read. The user can then enter a byte to be output to the port, followed by 'CR'. Subsequent 'CR's will display each port in turn, enter 'CR' if nothing is to be output. To cancel the command, enter '.' and 'CR'.

The command P 'CR' displays the complete port map.

2.2.9 COMMAND PS: - PRINTER SWITCH

After entering the command PS, all further information will be printed as well as displayed. A second PS command will cancel the function.



2.2.10 COMMAND S: - SET MEMORY

Example: S 4000

The entered start_address and its contents will be displayed.

4000 21

- original contents 21H

The contents can be altered [enter new value], or left unchanged [enter 'CR']. The next address will then be displayed. To cancel the command, enter '.'

4000 4001 4002 4003	00 50	10 CR	changes contentschanges contentsleaves contentschanges contents	to as	10H 50H
4003 4004			- cancels command	••	J

2.2.11 COMMAND SK: - SEEK STRING IN MEMORY

Example: SK CD F9 F6

All addresses where the string 'CD F9 F6' occur are displayed.

Maintenance Facilities



3 TERMINALBOARD TEST

After the port setup, the terminalboard attempts to send two characters to the mainboard and the mainboard should send them back. If this does not happen, the message SYSTEM ERROR! is displayed by the terminal program.

If the ESC key is pressed at the same time as the RESET, the ROM-resident terminal test program is activated. It has two parts: $\frac{1}{2}$

- 1. ROM Checksum Test
- 2. Simple RAM Test

If ready, the OK or the error message is displayed and in case of error, the test stops. If no error is found, the test is repeated continuously until a key is pressed (it is a very simple keyboard test). The normal terminal operation is then restored.

A more sophisticated terminalboard memory test can be loaded from the mainboard maintenance program.



Maintenance Facilities

MAINTENANCE PROGRAM

The following files constitute the Maintenance Program and will be present on the diskette which is part of the P2599:

MN11.COM MN11.OVL MTS.HEX MTL.HEX MTL100.HEX

The main part of the program is called MN11.COM (Version 1.1). It can be activated in the CP/M environment by typing MN11 and pressing the 'CR' key. This part resides in locations 100 to 2FFF. The second part of the program is MN11.OVL. It contains the extension tests and resides in locations 8000 to BFFF. To start the program, both parts must be present on the same disk. The MTS.HEX and MTL.HEX files contain the terminalboard memory test. The MTL100.HEX file contains information required for the terminalboard burn-in test.

At the very first loading of the program the self-configurating part is activated automatically (see 4.6) and the disk must be write enabled.

On start-up a menu is displayed with the following options:

- 1 MAIN TESTING PROGRAM
- 2 TERMINAL BOARD MEMORY TEST
- 3 HARD DISK TEST
- 4 MEMORY EXTENSION BOARD TEST
- 5 PARALLEL (IEC) BOARD TEST
- 6 RECONFIGURE MAINTENANCE PROGRAM
- 7 BURN-IN TEST
- 8 SHORT BURN-IN TEST

After executing any item except a memory test in the Main Testing Program, this menu is displayed again. After returning from the main testing program, if a memory test has been executed, the loading disk must be in the original drive (to reload CP/M and the overlay that have been destroyed during the memory test).

When a test is completed the results are displayed on the screen. If a printer is connected the results are also printed.

Note: The checksum is only calculated when a MEMORY TEST is carried out! Perform a MEMORY TEST (from the Main Testing Program) before carrying out any other test using MN11.



4.1 Main Testing Program

Selection of the Main Testing Program produces the following menu:

SELECT TEST:

- 1 MEMORY
- 2 DISK
- 3 KEYBOARD
- 4 SCREEN
- 5 PRINTER
- 6 BEEPER
- 7 SUMMARY
- 8 DEBUGGER

Each item is a sub-routine and after execution the menu will be displayed again.

4.1.1 1. MEMORY TEST

Within the memory test, the following options are offered:

MEMORY TEST:

- 1 SHORT
- 2 LONG
- 3 SHORT MEM-COMM-FLOPPY-TEST
- 4 LONG MEM-COMM-FLOPPY TEST

The short test gives a good indication of 'hard' memory errors within a few seconds.

The long test applies a stronger thermal load on the memory cells and can detect errors that are more difficult to find. The difference between the two tests is in the testing pattern and the test algorithm. In the combined tests (3 and 4) the memory test is followed by a very critical test for memory and DMA.

Before the test the checksum of the program range is computed. It is tested after each step of the test. In the event of an error, the following message is displayed:

'CHECKSUM ERROR IN SYSTEM RANGE, PROGRAM DAMAGED!!!'

and the program stops.



The testing procedure is as follows:

- a. The BIOS is shifted down (under 4000H).
- b. Locations 0 3FFF are shifted up to COOO FFFF
- c. Locations 0 BFFF are filled with the test pattern, checked, inverted and checked again.
- d. The range COOO FFFF is shifted down to 0 3FFF.
- e. The locations above 4000H are filled with the test pattern.
- f. The locations above 4000H are checked, inverted and checked again.
- g. The BIOS is restored.

During testing, the following characters are displayed:

F = filling; T = testing; I = inverting

For the combined test, the following procedure is added. The user should insert (scratch) testing disks into both drives.

A 'test' communications connector should be fitted, with the following interconnections:

$$[2-3]$$
, $[4-5]$, $[8-20]$, $[15-17-24]$

Note: This is different to previous versions, please check your connector.



h. The drives are checked for ready. If either drive is not ready, the program stops. Pressing any key will return to the main menu in 4.1. If a CP/M disk is inserted, the program asks:

DESTROY CP/M DISK? (Y/N)

The only answer that will be accepted is Y(es)! If you wish to retain your CP/M disk you may exchange it for another (scratch) disk or press RESET.

A character is then sent through the communications connector and checked for correct reception. In the event of an error, one of the following messages is displayed:

COMMUNICATION CONNECTOR (SHORTS: 2-3, 4-5, 8-20, 15-17-24) MISSING

or

WRONG DATA ON SIO

In either case the message is followed by two hexadecimal bytes displaying the SIO status and data registers respectively.

i. The SIO channel-A is programmed for DMA transfer and the memory with the test pattern is transferred through the communication connector to a 100H byte long temporary buffer. During the transfer the previously transferred block is recorded to disk and a text line is displayed:

COMMUNICATION AND FLOPPY WRITE

It means that all four channels of the DMA are active at the same time! For short test 16 blocks are transferred, for long tests 183 (decimal) blocks.

- j. The memory is checked.
- k. The disk is read back to the original locations (the message 'R' is displayed) and the memory is checked again.



To assist troubleshooting a special display format has been selected to summarize all error cases.

For example, suppose the following errors have been found:

Address	Expected	Read		
10101000 00000000 10101111 11111111	$\begin{smallmatrix} 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 & 1 & 0 & 1 & 1 \end{smallmatrix}$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$		

The resulting error message would be:

ERROR AT ADDRESS: 10101XXX XXXXXXXX BITS: 101XXXGG

The symbols summarise the condition of the corresponding bits:

0: if error found, the bit is always set at 0
1: if error found, the bit is always set at 1
X: if error found, the bit was set at 0 or 1
G: no errors found on this bit (always Good - only in DATA field)

The error message above has the following meaning:

Errors have been found in the range A800 to AFFF

When bits 7 & 5 were incorrect, they were always set to 1
When bit 6 was incorrect, it was always set to 0
When bits 2, 3 & 4 were incorrect, they were sometimes 1 and sometimes 0
No errors were found in bits 0 or 1

If any error has been detected, and the printer is not connected, the procedure stops. At 'no error', a wait loop of 10 seconds is started. During that time the user can discontinue testing by entering '0' (zero), otherwise the procedure is repeated.

Maintenance Facilities



4.1.1.1 Test Patterns

Short test: The first byte is 93. It is rotated one position left and written to the next address, and so on... One permutation (C9) is excluded to achieve a 7 byte cycle:

93, 27, 4E, 9C, 39, 72, E4

Long test: The first byte is a random number. The increment is the sum of this random number, a constant and the high and

low address bytes of the tested byte. The random number

is changed before each pass.

4.1.1.2 Test Algorithm

Short test: The byte is simply tested against the expected value.

Simple inversion is then carried out.

Long test: The byte is tested against the expected value, and then

rotated eight times. It is tested with each rotation. Inversion is carried out bit by bit and checked each

time.



4.1.2 2. FLOPPY DISK TEST

Within the floppy disk test, the following options are available:

FLOPPY DRIVE TEST:

- 1 READ MASTER FLOPPY
- 2 WRITE-READ TEST FLOPPY
- 3 COPY FLOPPY 1 2
- 4 COMPARE FLOPPIES

4.1.2.1 Read Master Floppy

The aim of this test is check the performance of the drives being tested to ensure that they can read a test pattern from a 'master floppy'. A master floppy will be part of a service engineers 'tool kit' and can only be generated on a well adjusted drive!

To produce your own, the floppy must first be formatted (using the UTIL program) and the test pattern then written using the Write-Read Test Floppy procedure as follows:

Write the complete disk and, when the program starts to read it, enter '0' to abort the procedure. Remove the disk from the drive and attach a write-protect label.

After selecting the 'Read Master Floppy' procedure, insert a master floppy in each of the drives that are to be tested and enter the corresponding drive numbers (1-4). Any combination of drive numbers 1 to 4 can be entered.

The following steps are then carried out:

- 1. Step to track-0 and check the 'track-0' and 'write protect' signals.
- 2. Step to highest track and check identifier.
- 3. Step to track-0 and check identifier.
- 4. Read all tracks from 0 upwards and evaluate the results. In case of error a sector by sector read is started up to two times for each sector. After each step the identifier is also read. The error messages are displayed and printed.
- 5. After the reading of the last track the next drive is tested. If all drives are ready, the first drive is tested again from point 3. The test pattern and the error messages are described under Write-Read Test Floppy.

Maintenance Facilities



4.1.2.2 Write-Read Test Floppy

Any combination of drive numbers 1 to 4 can be entered.

A formatted disk without 'WRITE PROTECT' label must be inserted in each of the specified drives.

The following steps are then carried out:

- 1. Step to track-0.
- 2. Write the test pattern (both sides), step to next track and repeat until the last track has been written.

When all tracks have been written with test pattern:

- 3. Read each track and check the test pattern from the highest track down to track-0.
- 4. Test the next drive.
- 5. When all selected drives have been tested, increment the pass number and test the first drive again.



Testing Pattern:

This is slightly different for each sector of the disk. The disks are written with double density; one sector has 256 bytes, one track has 16 sectors. The 160K disks are written on one side and 40 tracks, the 640K disks are written on both sides and 80 tracks each.

The test pattern for each sector is as follows:

Byte-0 and Byte-1: A random word, different for each writing pass

but the same for all sectors.

Byte-2: Number indicating drive and head number.

See Byte-2 in diagram below.

Byte-3: physical track-number

Byte-4: sector-number + 3FH (varies between 40 and 4F).

Byte-5 to Either:

Byte-255: DB 6D B6 DB 6D B6 DB 6D ...

or B6 DB 6D B6 DB 6D B6 DB ... or 6D B6 DB 6D B6 DB 6D B6 ...

depending on the remainder of RANDOM/3.

The relationship between the disk drives (1 & 2 internal and 3 & 4 external) and the disk 'sides', the logical drive numbers and the contents of Byte-2 in the test pattern is shown in the following diagram:

I	NT • • •	EX	т	
1	2	3	4	Physical Drive Number
0 1		1 1	0 1	Disk 'Side'
1 5	2 6 	3 7 	4 8 	Logical Drive Number (Head)
0 4	1 5	2 6 	3 7	Byte-2



Error Messages:

The message line is built up as follows:

where:

[##.] is a count of the passes

[drn] is the logical drive (head) number

[ST] means STEP (followed by 'read identifier')

[RD] means READ

[WR] means WRITE

[#] following TR- is the track number; at sector read the track number is extended by 'S' + sector number (1 to 16).

[n] is the error repetition number (1 or 2)

[error text] is a short description of the error.

Note: If a message with '!' appears, it means wrong data without any error message from the disk controller.

[7 HEX bytes] are the 'result bytes' from the uPD765 disk controller [E] means Error Summary where:

[nl] is the total number of aborted track operations

[n2] is the total number of detected errors

An expansion of the 'short' error texts is given below:

ABNORM TERM: Execution of a command was started but not

successfully terminated.

BAD TRACK: The track number stored on the diskette is FF.

CRC ERROR: FDC detected a checksum error in data field.

DELETED DATA: A sector with deleted data address mark is found.

END OF TRACK: FDC tries to access sector beyond the final sector

of the cylinder.

FAULT: The Fault signal is received from the FDC.

IDNT CRC ERROR: Checksum error is found in the sector identifier.

NO DATA: FDC cannot find the specified sector.



NO ADDR MARK: FDC cannot find either Identifier Address Mark or

Data Address Mark.

NO TRACK-0: The Track-0 signal fails to appear after 77 steps

during the RECALIBRATE command.

NO WRITE The master diskette at 'READ MASTER DISK' has no PROTECTION: write protection label.

I WOIDOILON.

DRIVE NOT READY: The FDC is in the 'NOT READY' state and a read or

write command is issued.

UNIT SELECT ERR: Response from a unit that has not been selected.

WRITE PROTECT: During write, FDC detects a write protect signal.

WRONG SIDE: The Side Select Signal of the drive is incorrect.

WRONG TRACK: The track number stored on the diskette differs

from the expected number.

RANDOM DATA ERR!: The Random Data of a sector (byte-0 and byte-1) is

incorrect.

DRIVE DATA ERR!: The Drive data in a sector (byte-2) is incorrect.

TRACK DATA ERR!: The Track data in a sector (byte-3) is incorrect.

SECT DATA ERR!: The Sector data in a sector (byte-4) is incorrect.

WRONG DATA!: The DB, 6D, B6, DB ... pattern (bytes 5 - FF) is

incorrect.

If the controller does not finish the read or write track operation within 616 ms the 'DISK NOT READY' message is displayed and the user has to press a key to return to the disk test menu. Such an error can occur if:

- no disk is inserted

- the drive is not connected or is defective

 the READ DATA line on the floppy drive bus is disturbed and the synchronization before some sectors cannot be achieved within the specified time.

Maintenance Facilities



4.1.2.3 Copy Floppy 1 to 2

The disk in drive 1 is copied to drive 2, regardless of data. Data is read track-by-track but in the event of an error each sector of the track is re-read up to two times in an attempt at error recovery. After copying, the copy is verified.

4.1.2.4 Compare Floppies

The disks in drives 1 and 2 are verified on a track-by-track basis. The number of deviations (if any) is displayed and printed.



4.1.3 3. KEYBOARD TEST

At the keyboard test a figure showing the keyboard is displayed. One key (starting with the top left) is inverted and the user should press the inverted key. If OK, the next one is displayed, otherwise the beeper sounds and the expected and received codes are displayed. If a key input is incorrect 5 times, the corresponding symbol is underlined and the next key is asked for. If no key is pressed within 4 seconds the question 'CONTINUE? (Y/N)' is displayed. After 'Y' the test is continued, after 'N' a printout is made where all faulty keys are marked (keyboard error map).

The P2000C mainboard software has no access to the keyboard position codes, only the converted ASCII codes can be input. For this reason, some special keys (lock, shift, control, supershift) cannot be checked individually. These special keys are checked together with an auxiliary key. Both keys are inverted on the display. The special key must be pressed and held and the auxiliary key then pressed.

If all keys are ready, an OK message or the keyboard error map is printed (if an error has been found).

4.1.4 4. SCREEN TEST

Within the screen test, the following options are available:

- 1 ALPHANUMERIC
- 2 GRAPHICS
- 3 HIGH RESOLUTION GRAPHICS
- 4 SCREEN ADJUSTMENT
- 5 SPECIAL FEATURES

4.1.4.1 Alphanumeric Test

A test figure containing 23 lines with 23 different alphanumeric characters (each line has the same character 80 times) is displayed and an instruction to type any key. It is repeated until all alphanumeric characters are displayed. At the end the user must qualify the result (OK or not).



4.1.4.2 Graphics (Mosaic Graphics) Test

Two pictures are generated, each containing all graphics characters. Both pictures are symmetric and the second one is the inverse of the first. The user must qualify the figures.

4.1.4.3 High Resolution Graphics Test

Two pictures are shown, the first with 256 x 252 dots and, after pressing any key, the second with 512×252 dots. Both display an 'X' shape with a (logical) circle in the middle. The user must qualify the result.

4.1.4.4 Screen Adjustment Test

A figure is displayed where lines and columns of letter '0' divide the picture into 4×4 equal parts to check the linearity. All other character positions are filled with '.'. In addition, the edges are inverted to show the screen adjustment clearly. WARNING: The last position in the last line is not displayed to avoid scrolling up. The user must qualify the result.

4.1.4.5 Special Features

The screen is inverted and six lines with the letter 'A' are displayed. Alternate letters have the 'special' feature:

1st line: Underline
2nd line: Quarter bright
3rd line: Half bright
4th line: Bold
5th line: Inverted
6th line: Flashing

The user must qualify the picture.



4.1.5 5. PRINTER CHARACTER TEST

If the printer is not ready, the beeper sounds. If any key other than '0' (zero) is pressed the ready bit is checked again. If the printer is found to be ready the test is started. Pressing the key '0' aborts the test.

The print character test is a simple test for all printable characters. Six lines are displayed with the following characters:

20-3F, 40-5F, 70-7E, A0-BF, CO-DF, E0-FE

The program fully considers the printer translation table of the booting system disk.

Afterwards a 'print screen test' is made with 8 shifted lines. If the terminalboard sends all the expected characters, the 'PRINT SCREEN TEST OK' message is sent.

If too many characters have been sent, the message 'TERMINAL BOARD ITEM 7406 USART-8251 IS DEFECTIVE!' is displayed. The indicated circuit must be replaced by any of the following types:

Type	Manufacturer		
INS 8251N COM 8251	National Semiconductor		
D8251A	Intel		
NEC D8251AFC	NEC		

4.1.6 6. BEEPER TEST

The beeper sounds periodically until the user presses a key and qualifies the beeper.

4.1.7 7. SUMMARY

The summary has the following format:

SERIAL NUMBER: (user entry)
NATIONAL VERS: NL/UK (or other) according to users' answers in
FLOPPY DRIVES: 640K (or 160K) the configuration menu

DATE: (user entry)
INSPECTED BY: (user entry)

If a printer is connected, the summary is printed.



4.1.8 8. DEBUGGER

The debugger in the IPL ROM is called (see section 2.2) and the user can observe the memory or disk contents. On entry a line is displayed:

RETURN TO MAINTENANCE with: G xxxx

where xxxx is a 4 character hexadecimal address.

The user MUST NOT CHANGE any memory contents except 4000 to 7FFF, otherwise the maintenance program is corrupted and CANNOT BE REUSED after return.

4.2 Terminal Board Memory Test

The actual tests are in the MTS.HEX and MTL.HEX files, which must be present on the loading disk.

The following menu will be displayed:

TERMINAL BOARD MEMORY TEST

1 - ONE PASS

2 - ENDLESS

The file MTS.HEX or MTL.HEX is loaded into memory and then into the terminal board with the 'LOAD INTEL HEX FILE' feature.

The RAM in the terminalboard is checked in two parts:

Range 1: COOOH - FFFFH Range 2: 8000H - BFFFH

Each range is written with the test pattern and checked 256 times. In case of error the address is displayed and the beeper activated.

In the short test the procedure is carried out 3 times, after which the terminal board is reset. In the long test, the test runs continuously until the RESET button is pressed.



4.3 Hard Disk Test

4.3.1 GENERAL TEST PHILOSOPHY

Make sure that the jumper on the controller card is set to 256 bytes/sector.

The hard disk should be formatted (using UTIL) before testing.

The individual testing routines send different commands to the XEBEC controller and in case of error the reason is asked (if possible). A single command has the following structure:

- 1. Define timeout for the operation.
- 2. If 'BUSY' bit active:
 'XEBEC CONTROLLER NOT READY'.
- 3. Make 'select' for the controller. If BUSY is still inactive: 'BUSY INACTIVE AFTER SELECT'.
- 4. Send command. Repeat the following procedure 6 times:
 If REQUEST bit inactive within specified time:
 'COMMAND NOT FETCHED BY XEBEC', else send command byte.
- 5. Command is executed. Get status byte. If MESSAGE and REQUEST bits are not active within timeout: 'FIRST STATUS BYTE NOT RECEIVED'. This is the case when the sector size jumper is incorrect.
- 6. Get 'null byte'. If REQUEST bit inactive within timeout: 'SECOND STATUS BYTE NOT RECEIVED'.
- 7. Check DMA address register. If data transfer incomplete (due to hardware error on handshake lines):
 'DATA TRANSFER ON DMA TOO SHORT'.
- 8. If bit-1 of the status byte (see 5) is 1, make a 'Request sense status' command to check the reason for the error and the accurate disk address of it.



The following messages are possible:

NO INDEX DETECTED FROM DRIVE NO SEEK COMPLETE FROM DRIVE WRITE FAULT FROM DRIVE DRIVE NOT READY (after selection) NO TRACK-O (found after recalibrate) IDNT CRC ERROR (read error in identifier field) UNCORRECTABLE DATA ERROR NO ADDRESS MARK (address mark not found) Note: This message appears when two drives with the same jumpering are connected to the XEBEC controller. TARGET SECTOR NOT FOUND SEEK ERROR CORRECTABLE DATA ERROR ILLEGAL DISK ADDRESS BAD TRACK FLAG DETECTED FORMAT ERROR RAM BUFFER FAILURE PROGRAM MEMORY CHECKSUM ERROR ECC DIAGNOSTIC FAILURE

9. If a test pattern is read, the following structure is expected on each sector:

Byte-0 and Byte-1: A random word, different for each pass.

Byte-2: FF for drive-0 or FE for drive-1

Byte-3: Logical address HIGH on the disk

Byte-4: Logical address MIDDLE on the disk

Byte-5: (Logical address LOW on the disk) AND OCO

Byte-6: Buffer address HIGH (40 to 9F)

Byte-7 to Either:

Byte-255: DB 6D B6 DB 6D B6 DB 6D ...

or B6 DB 6D B6 DB 6D B6 DB ... or 6D B6 DB 6D B6 DB 6D B6 ...

depending on random data in byte-0.

Errors in the test pattern will result in the following messages:

RANDOM DATA ERROR!: error in bytes 0 or 1

DRIVE DATA ERROR!: error in byte 2

TRACK DATA ERROR!: error in bytes 3, 4 or 5

SECT DATA ERROR!: error in byte 6

WRONG DATA!: error in bytes 7 to FF



4.3.2 SELECTABLE TESTS

The following tests are available:

XEBEC CONTROLLER INTERNAL DIAGNOSTICS SELECT DRIVE AND SHORT TEST DRIVE READ ONLY TEST DRIVE WRITE-READ TEST

4.3.2.1 XEBEC Controller Internal Diagnostics

The controller checks its internal processor, data buffers, ECC (error detection and correction) circuits, the checksum of the program memory and a diagnostics on the RAM buffer. No drive is accessed. The test is repeated until the '0' key is pressed.

4.3.2.2 Select Drive and Short Test

At first the user is warned that the system tracks on his hard disk will be lost but no files will be damaged. Then he has to select the drive (1 or 2). It is assumed that the drive is correctly formatted. The selected drive and drive-to-controller interface is tested. The controller sends recalibrate and seek commands to the selected drive and verifies sector 0 of all the tracks on the disk. Afterwards a write-read test is performed on the first 8K of the disk. Finally the alternative drive is read and if the same contents is found a warning is displayed saying that the same disk hangs on drive 1 and 2. It is not a serious error if only one disk is attached to the controller (the drive select jumper on the drive is not set properly).

If no error has been found the following message is displayed (for 10MB hard disk):

DIAGNOSTICS OF DRIVE 1 DISK ADDRESS 009900 OK SHORT WRITE-READ TEST OK

The displayed hexadecimal disk address gives the disk capacity in sectors (256 bytes). In the case of a 5MB hard disk its value is 004C80.



4.3.2.3 Drive Read Only Test

The data is read continuously from the hard disk drive selected using the 'SELECT DRIVE AND SHORT TEST' procedure (or from drive 1 if nothing has been selected). If the last track is reached, the procedure starts again until the '0' key is pressed. In case of error, the address of the faulty sector is displayed together with an error text.

4.3.2.4 Drive Write-Read Test

The user is warned that this procedure destroys ALL data on his hard disk and he can continue only after typing 'YES'. Each sector of the disk is written with a unique test pattern. When the disk is full its contents is checked and the procedure is repeated until the 'O' key is pressed. Afterwards 'E5H' is written to each byte of the first 16K of the hard disk. In the case of the 10 MB hard disk it is recommended to format the disk again because the directory in the higher part of the hard disk will not be cleared by E5.

4.4 Memory Extension Board Test

The program first checks that a memory Extension Board is fitted. If not, the message 'WRONG BOARD' is displayed.

The program checks the memory quality as well as the bank and cache

switching properties of the P 2092 memory extension board.

Two tests are available: SHORT and LONG.

Memory Write-Read Test

According to the user selection either the short or the long test is carried out. In the short test a simple rotating pattern is used and the testing is a simple byte check. The long test uses a quasi-random pattern and during testing the byte is rotated 8 times and checked each time. Both of them execute a memory write-read test and a bank switching test.



Before the actual test the checksum of the $0-7 {\rm FFF}$ range of the system RAM is recorded and checked after each testing stage. In the event of an error in this check a message is displayed:

CHECKSUM ERROR IN SYSTEM RANGE, PROGRAM DAMAGED!!!

and the program halts. It means that during a memory write to the extension RAM the system RAM has been also been written.

The test is carried out in the cache mode. During testing a letter is shown indicating the procedure in progress:

F : Fill extension memory with the testing pattern

T : Test a cache (16 times)
I : Invert a cache (16 times)

T : Test the inverted pattern (16 times)

The error message format (printed and displayed) is as follows:

22.PASS BANK-1 (IC:7014-7021) ADDRESS: 10XXXXXXX XXXXXXXX BITS: 011GGXXG

where: the number preceding PASS is the pass number

BANK = 1..4 and indicates the faulty page number. It is
followed by the IC position range of the corresponding bank.

The symbols in the BITS fields represent the condition of the bits within the range indicated by the two address bytes:

0: if this bit is wrong, it is always set at 0

1: if this bit is wrong, it is always set at 1

X: if this bit is wrong, it was set at 0 or 1

G: no errors found on this bit (always Good)

The example shows that when testing BANK-1, errors were found in the range 8000H to BFFFH. These errors were:

all errors in bit 7 - bit set to 0
all errors in bits 6 & 5 - bit set to 1
errors in bits 1 & 2 - sometimes 0, sometimes 1
No errors were found in bits 0, 3 or 4



Bank Switching Test

If no error is found in the memory write-read test, a bank switching test is carried out.

The system memory bytes at the addresses of 0002, 4002, 8002 and C002 are saved and the program is multiplied to all banks in the WRITE-ALL mode. (If this mode does not work, the program hangs without any message because there is no other way to test the switching mechanism).

Then each cache (16K byte unit) is marked on byte-2 with a specific number (08, 18, \cdots F8). The possible switching modes (CROMIX, MP/M and OASIS) are activated and each cache is checked against the specifications.

The recorded addresses in the normal system RAM are then checked. Afterwards the marked byte of each cache is checked in CACHE-MODE as well as the 0 cache that is always active in the 0-3FFF range.

If any of these tests fail, the whole switching map is displayed showing the expected and received values. The bytes with error are inverted. As the whole map is longer than one page the second part is displayed after typing any key. The next keyboard entry returns to the main menu, and no further testing takes place.

After a successful test the program stops and waits about 5 seconds. If the user types '0' during this time (or has done so during the test), the program returns to the selection menu. Otherwise the test is repeated.

4.5 Parallel (IEC) Board Test

The program first checks that a memory extension board is NOT fitted. If it is the 'WRONG BOARD' message is printed and the test is not executed.

The reserve CTC channel (CTC2+2) is enabled for interrupts.

The selection menu is then displayed:

SELECT PARALLEL (IEC) BOARD TEST

- 1 STANDARD TEST
- 2 CONTINUOUS TEST WITHOUT PLUG
- 3 CONTINUOUS TEST WITH PLUG



4.5.1 STANDARD PARALLEL (IEC) BOARD TEST

A test is first carried out with an empty socket. All 65536 combinations are written to the output ports and read. In case of error, an error message is displayed with the following format:

DATA 7 6 5 4 3 2 1 0 CONTROL 7 6 5 4 3 2 1 0 GOOD:0,1 BAD:L,H FO 0 0 0 0 1 1 1 1 1 67 1 H H L L 0 0 0

This should be interpreted as follows:

It says that the byte FO has been applied to the data port and there is no error (the displayed bit values can be measured on the connector). The byte 67H has been applied to the control port where bits 6 & 5 are HIGH (instead of LOW) and bits 4 & 3 are LOW (instead of HIGH). Consider that the output bits are inverted!

The test continues with a user selected input:

O-QUIT 1-REPEAT 2-CONTINUE 3-SCOPE

Selections 0, 1 & 2 are self explanatory; 3 leads to the choice:

O-QUIT 1-READ 2-WRITE

If 1 or 2 are entered a further selection is required:

PORT: 0-QUIT 1-CONTROL 2-DATA

The user can thus select a continuous READ or WRITE test on the CONTROL or DATA port.



If WRITE has been selected, up to 10 hexadecimal bytes can be entered. After 'CR', the user can check the board with an oscilloscope.

Pressing any key will stop the procedure and return to the:

QUIT-READ-WRITE menu.

After the test with an empty socket, the user has to connect a simple IEC socket with the following interconnections:

$$[1-5]$$
, $[2-6]$, $[3-7]$, $[4-8]$, $[13-10]$, $[14-9]$, $[15-11]$, $[16-17]$

This connector makes a logical AND between the corresponding bits of the two output ports. (From the processor side it is a logical OR because of the inversions). When the connector is fitted and any key is pressed, the test is repeated.

During the test the number of CTC interrupts is counted and at the end a message indicates if the count was too high or too low.

4.5.2 CONTINUOUS TEST WITHOUT PLUG

All the 65536 combinations are written to the two output ports and the input ports are checked. The error procedure is the same as with the Standard Parallel (IEC) Board test. If ready a '.' is displayed and a new run is started until any key is pressed.

4.5.3 CONTINUOUS TEST WITH PLUG

The same procedure is carried out in this test, the difference being in the expected results due to the interconnections.



4.6 Reconfigure Maintenance Program

A menu is displayed with the supported national versions:

SELECT NATIONAL VERSION:

CH-D = Switzerland German
CH-F = Switzerland French
D/A = Germany and Austria

E = Spain

F/B = France and Belgium

[= Italy

NL/UK = Netherlands and United Kingdom

S/SF = Sweden and Finland

After national version selection, the following message is displayed:

Define disk configuration (1=160K, 2=640K, 3=not existing) INTERN:

EXTERN:

For example:

Define disk configuration (1=160K, 2=640K, 3=not existing)

INTERN: 1 (defines drives 1 & 2 as 160K) EXTERN: 2 (defines drives 3 & 4 as 640K)

Finally, the printer speed has to be selected from the following:

1 - 1200

2 - 2400

3 - 4800

4 - 9600

5 - 19200

This printer speed overwrites that set by the CP/M system.

The information entered during this program is written back to the disk. Therefore the disk must not be removed until the selection menu is displayed again.

Information supplied by the user is considered in the keyboard, screen, disk and printer tests.

Maintenance Facilities



4.7 Burn-in Test

This test procedure is designed for factory testing and will not be described in this document.

4.8 Short Burn-in Test

This test procedure is designed for factory testing and will not be described in this document.